# Exhibit 4

# United States Patent [19]

**Sasson et al.**

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[54] **ELECTRONIC STILL CAMERA UTILIZING IMAGE COMPRESSION AND DIGITAL STORAGE**


[75] Inventors: **Steven J. Sasson**, Hilton; **Robert G. Hills**, Spencerport, both of N.Y.

[73] Assignee: **Eastman Kodak Company**, Rochester, N.Y.



[21] Appl. No.: **349,566**

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[51] **Int. Cl.**[5] ..... **H04N 5/225**; H04N 5/30

[52] **U.S. Cl.** ..... **358/209**; 358/909; 358/906; 358/961.3

[58] **Field of Search** ..... 358/479, 906, 909, 261.3, 358/427, 229, 335, 209; 360/32, 35.1



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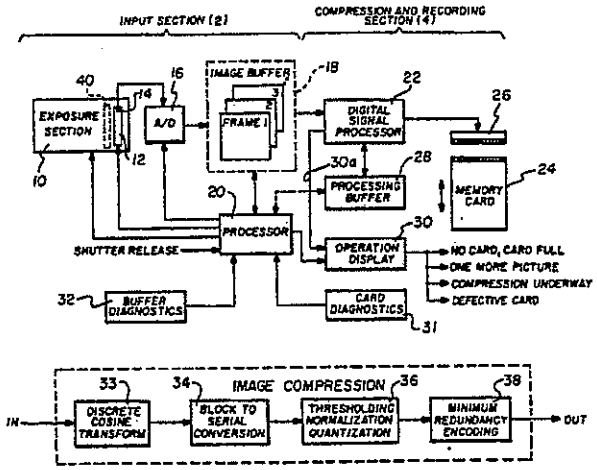
*Primary Examiner*—James J. Groody
*Assistant Examiner*—Kim Yen Vu
*Attorney, Agent, or Firm*—David M. Woods



[57] **ABSTRACT**

An electronic still camera employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable static random access memory card. An image sensor is exposed to image light and the resultant analog image information is converted to digital image signals. A control processor controls the exposure section and the A/D converter, delivering digital signals to a multi-image buffer at a rate commensurate with normal operation of the camera. A digital processor operates on the stored digital signals, transforming blocks of the digital signals and encoding the signals into a compressed stream of processed image signals, which are downloaded to the memory card. The digital processor operates at a throughput rate different than the input rate for better image capture and optimum utilization of the camera.


**18 Claims, 5 Drawing Sheets**



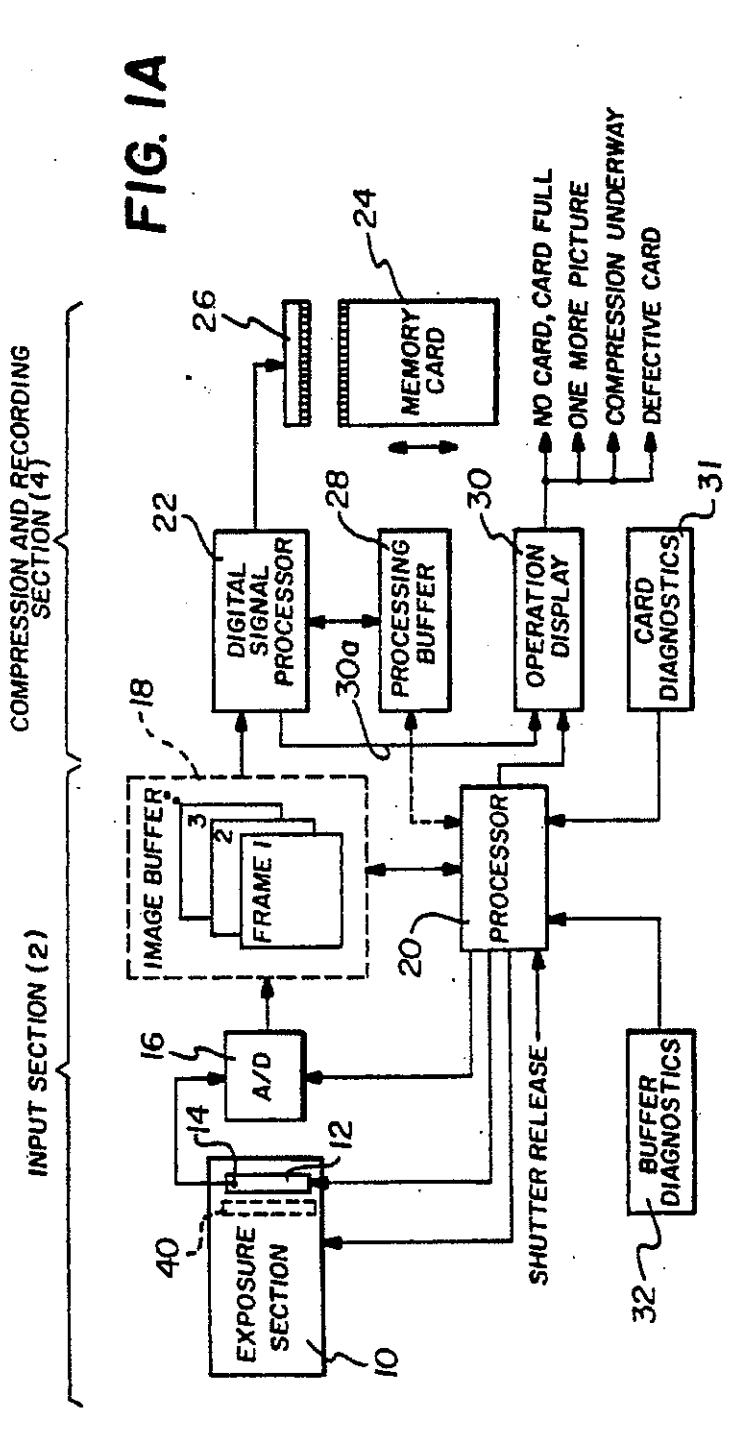


FIG. 1A
COMPRESSION AND RECORDING SECTION (4)
INPUT SECTION (2)
IMAGE BUFFER
FRAME 1
EXPOSURE SECTION
A/D
DIGITAL SIGNAL PROCESSOR
PROCESSING BUFFER
PROCESSOR
OPERATION DISPLAY
CARD DIAGNOSTICS
BUFFER DIAGNOSTICS
MEMORY CARD
SHUTTER RELEASE
NO CARD, CARD FULL
ONE MORE PICTURE
COMPRESSION UNDERWAY
DEFECTIVE CARD
10
12
14
16
18
20
22
24
26
28
30
30a
31
32
40

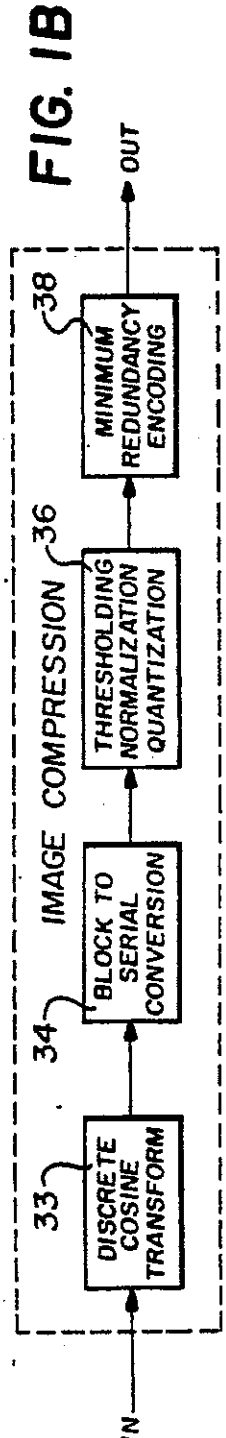


FIG. 1B
IMAGE COMPRESSION
IN
OUT
DISCRETE COSINE TRANSFORM
BLOCK TO SERIAL CONVERSION
THRESHOLDING NORMALIZATION QUANTIZATION
MINIMUM REDUNDANCY ENCODING
33
34
36
38

AX203263

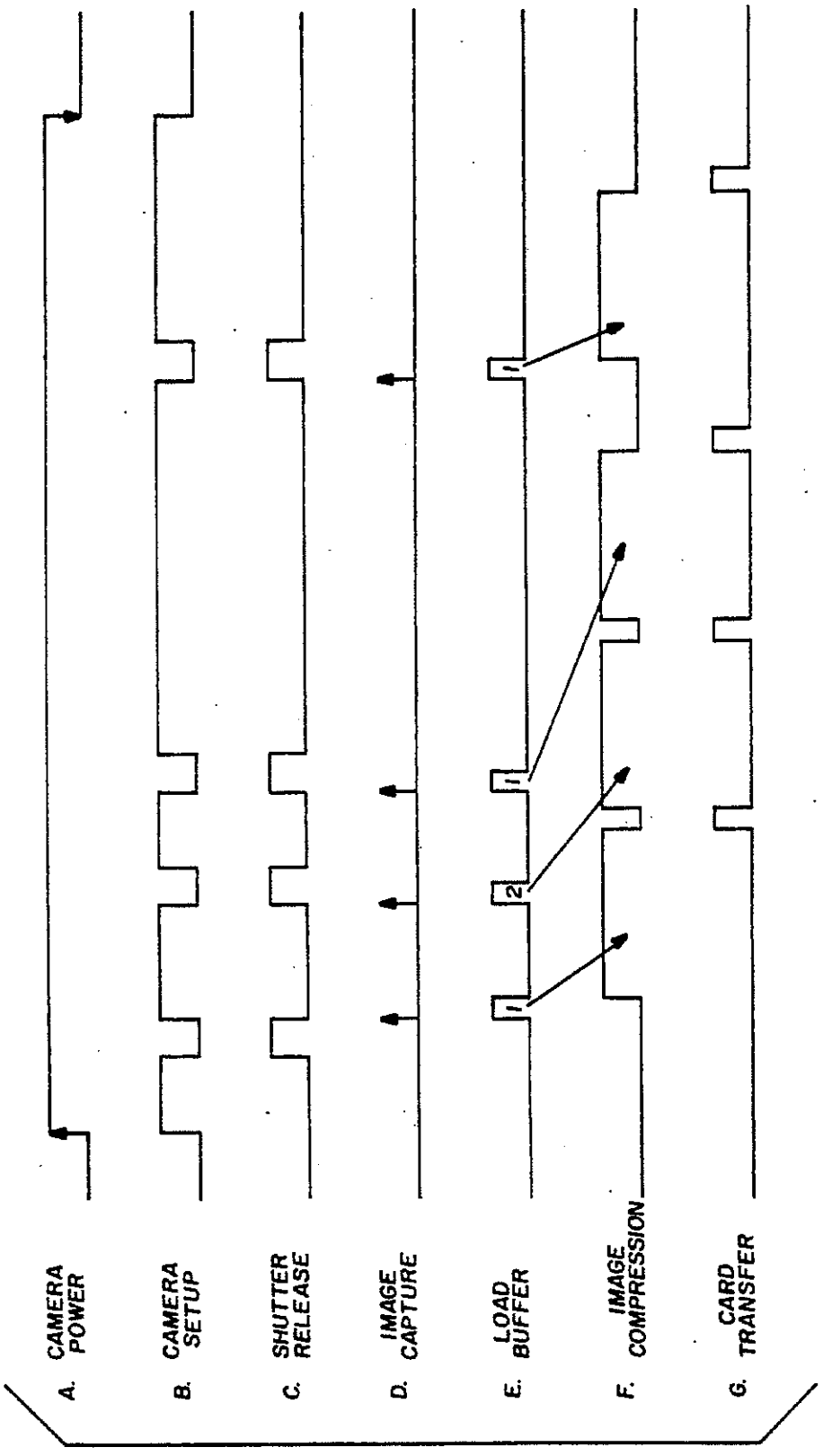

A. CAMERA POWER
B. CAMERA SETUP
C. SHUTTER RELEASE
D. IMAGE CAPTURE
E. LOAD BUFFER
F. IMAGE COMPRESSION
G. CARD TRANSFER
1
2
1
1

FIG. 2A

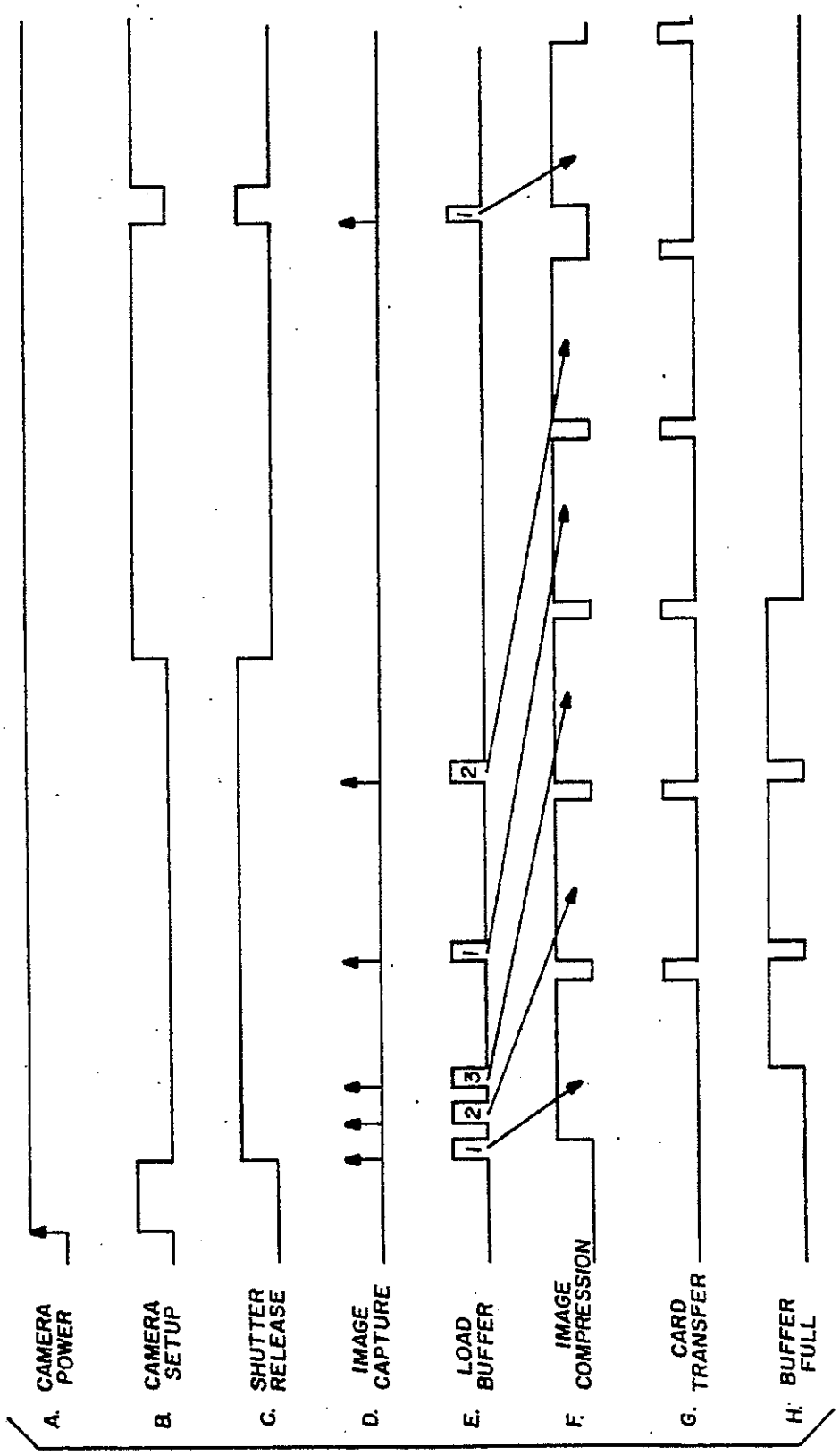



FIG. 2B

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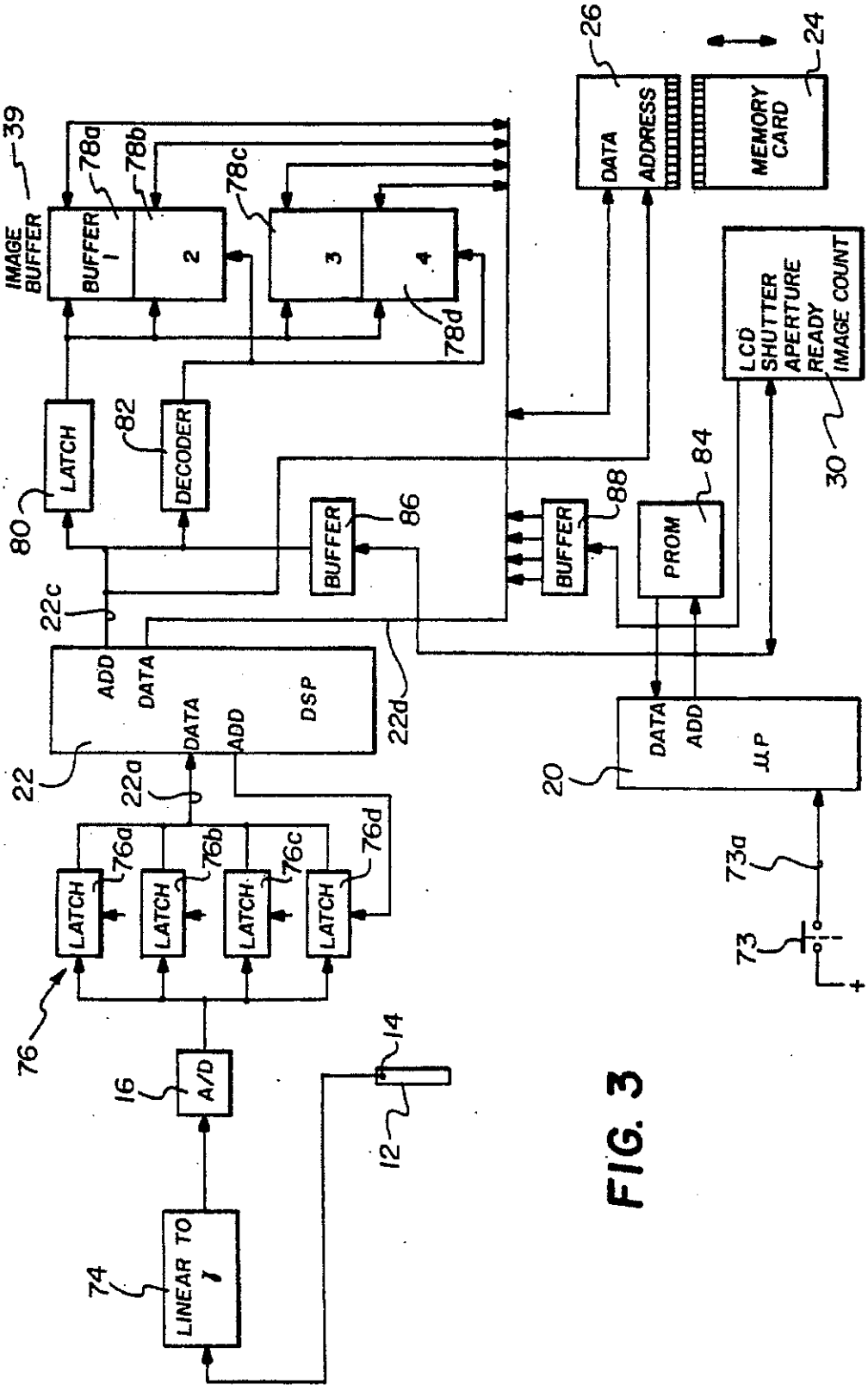


FIG. 3

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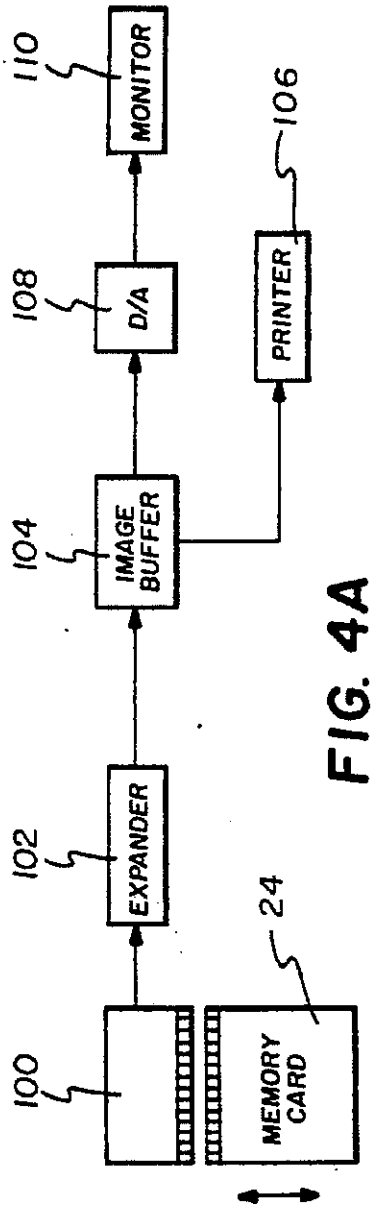


FIG. 4A

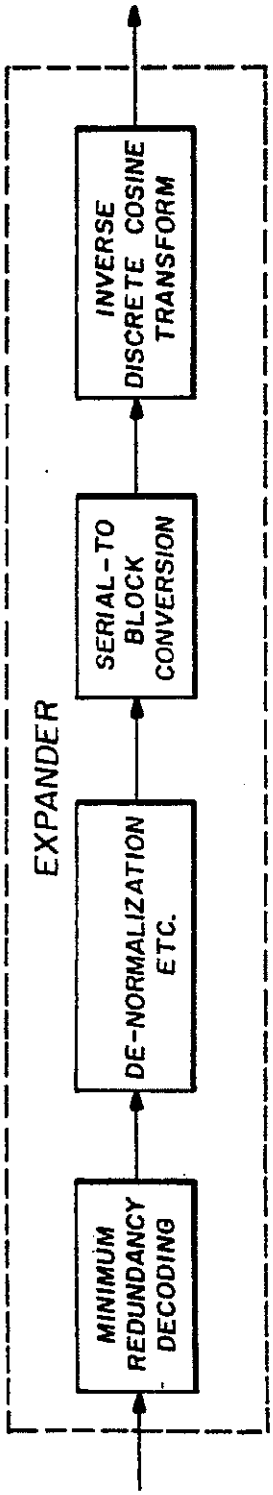


FIG. 4B

AX203267

# ELECTRONIC STILL CAMERA UTILIZING IMAGE COMPRESSION AND DIGITAL STORAGE

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains in general to the field of electronic still imaging and, more particularly, to an electronic camera incorporating digital processing of image signals derived from an electronic image sensor and digital storage of the processed signals in a removable storage medium.

2. Description Relative to the Prior Art

An electronic still camera employing non-volatile storage of digital image signals is described in U.S. Pat. No. 4,489,351. Analog color information from three charge-coupled device (CCD) image sensors is converted into a digital bit stream and transmitted through a peripheral memory control unit to an integrated circuit memory. The memory is one unit of many, e.g., twenty-four memory units, recessed into a "cassette" that is separably attached through an electrical connector to the camera body. In order to obtain a digital image of high quality, many pixels, and thus many bits of digital information, need to be processed in a short time. In an article entitled "Possibilities of the Digital Electronic Still Camera", by Sumihisa Hashiguchi (*Shashin Kogaku*, pp. 110–111, Feb. 1988), the author proposes a multi-layer image processing integrated circuit including sensors, analog-to-digital (A/D) converters, and 8-bit buffer storage cells in respective layers. Since the output signal from an individual pixel is transferred "vertically" through an A/D converter to an included storage cell, real-time throughput is obtained without high speed operation. The stored signals can be read out slowly for digital recording, perhaps after compression, on a storage drive incorporating a small floppy disk. (Another example of a digital-based electronic still camera is shown in published UK Patent Application 2089169, in which the camera loads the digital image signals into a bubble memory cassette.)

A static random access memory (SRAM) card, in the size, and form, of a credit card, is an attractive storage alternative to the devices described in the above-related disclosures. For instance, published European Patent Application 289,944 shows a detachable SRAM module for use in a digital electronic still camera. The module is disclosed as a 32 M-bit (4 M-byte) SRAM integrated circuit card, although such storage capacities in a card are not commonly available at this time. A 512 K-byte SRAM card is presently available (Mitsubishi Electronics America, Inc. is one supplier). However, as pointed out in an article by Sumihisa Hashiguchi ("Picture Recording and Electric Power Consumption," *Shashin Kogyo*, pp. 94–95, Apr. 1988), there is a significant problem with memory volume. In the case, for example, of recording 780×490 picture elements from a CCD image sensor, with 8 bits allocated to each picture element, 382,200 bytes are required for a single monochrome video frame. This amounts to only one picture on a memory card (of 512 K-bytes). This is a considerable obstacle since still photographers are used to taking many pictures, e.g., 24 or 36 pictures, with one cassette of conventional film. Moreover, color pictures would ordinarily require three times the storage capacity of monochrome pictures.

Dynamic random access memory (DRAM) offers more storage in a reasonable volume, but power consumption quickly becomes formidable as storage capacity increases. The Hashiguchi article, consequently, calls for the development of new techniques of storage based on the compression of picture information by a factor of 10 or 100. As Hashiguchi points out, several picture compression techniques are available at present. For example, the aforementioned European Patent Application 289,944 suggests an embodiment in which a signal processor is adapted to accomplish data compression, such as the Hadamard transform, cosine transform or orthogonal transform, and coding on the video signal, which in turn is transferred to and stored interest that U.S. Pat. No. 4,131,919, which issued on Dec. 26, 1978, proposes the use of source and/or channel encoding schemes to more efficiently record digital still image signals on magnetic tape.) Adaptive differential pulse code modulation is another known compression algorithm for encoding still images.

The fundamental structure for in-camera digital processing is ordinarily based on a conventional analog camera, with digital processing techniques being applied to the functional analog blocks, such as color separation, white balance, gamma correction, and so on. This conventional transposition extends to real-time processing in that in-camera digital processing seeks, insofar as possible, to emulate real-time analog processing rates by rapidly accessing the imager, processing the resultant image signals, and writing the processed image signals to memory within normal video frame rates. (. . . albeit, that in the aforementioned *Shashin Kogaku* article of Feb. 1988, in U.S. Pat. No. 4,489,351, and in UK Patent Application 2089169, a buffer or temporary memory is provided to allow transmission of the image data to the recording device at a desired rate, which due to device or other limitations is often less than the image capture rate.) Nonetheless, as recognized by the Hashiguchi article, the available techniques neither adequately meet the requirement for real-time processing as needed by an electronic still camera nor the requirement for simply including the compression hardware with the camera.

## SUMMARY OF THE INVENTION

The problem with the available techniques is their focus on real-time throughput. The present invention departs from this focus by distinguishing the input function of the camera from the processing function so that, on the one hand, image signals from a plurality of still images accumulate at a rate commensurate with normal operation of the camera while, on the other hand, the accumulated image signals are digitally processed at a throughput rate different than the accumulating rate. The prior techniques tend, by nature of their focus upon speed, not only to direct compression choices to those capable of handling a data stream at an extremely fast rate, such as differential pulse code modulation (DPCM), but also tend to focus processing upon one image at a time. By providing a multi-image input buffer and separating digital processing from input requirements, the digital processor not only has more time to operate on blocks of image signals, in particular transform encoding the blocks of signals, but also obtains such processing advantages without disturbing the "stacking up" of images in the input buffer. The invention further utilizes a removable digital storage means, such as a SRAM memory card, to store the compressed image signals. With 10:1 compression, for example, the

byte requirement for a picture can be reduced by a factor of ten and many more images can be stored in the memory card.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, in which:

FIG. 1A is a block diagram of an electronic still camera employing digital processing according to the invention;

FIG. 1B is a block diagram of an exemplary form of image compression used in connection with the invention;

FIG. 2A is a functional sequence diagram showing multi-image input buffering;

FIG. 2B is a further functional sequence diagram showing full utilization of the input buffer and concomitant delay;

FIG. 3 is a block diagram showing details of a specific processing architecture for the electronic still camera;

FIG. 4A is a block diagram of an electronic still player for use in reproducing pictures taken with the camera of FIG. 1A; and

FIG. 4B is a block diagram of an exemplary form of image expansion used in connection with the player of FIG. 4A.

## DETAILED DESCRIPTION OF THE INVENTION

Because electronic still cameras employing charge-coupled device (CCD) sensors are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIGS. 1A and 1B, an electronic still camera is divided generally into an input section 2 and a compression and recording section 4. The input section 2 includes an exposure section 10 for directing image light from a subject (not shown) toward an image sensor 12. Although not shown, the exposure section 10 includes conventional optics for directing the image light through a diaphragm, which regulates the optical aperture, and a shutter, which regulates exposure time. The sensor 12, which includes a two-dimensional array of photosites corresponding to picture elements of the image, is a conventional charge-coupled device (CCD) using either well-known interline transfer or frame transfer techniques. The sensor 12 is exposed to image light so that analog image charge information is generated in respective photosites. The charge information is applied to an output diode 14, which converts the charge information to analog image signals corresponding to respective picture elements. The analog image signals are applied to an A/D converter 16, which generates a digital image signal from the analog input signal for each picture element.

The digital signals are applied to an image buffer 18, which is a random access memory (RAM) with storage capacity for a plurality of still images. The arrangement for allocating memory space in the image buffer 18 to individual frames may vary; for this description, however, the frames will be allocated to specific, identifiable memory spaces such that a new frame can be directly written over an old frame without affecting the other frames in the buffer 18. This, as will be shown, becomes convenient in unloading the buffer 18 and freeing memory space for a new frame as soon as the older ones are processed.

A control processor 20 generally controls the input section 2 of the camera by initiating and controlling exposure (by operation of the diaphragm and shutter (not shown) in the exposure section 10), by generating the horizontal and vertical clocks needed for driving the sensor 12 and for clocking image information therefrom, and by enabling the A/D converter 16 in conjunction with the image buffer 18 for each signal segment relating to a picture element. (The control processor 20 would ordinarily include a microprocessor coupled with a system timing circuit.) Once a certain number of digital image signals have been accumulated in the image buffer 18, the stored signals are applied to a digital signal processor 22, which controls the throughput processing rate for the compression and recording section 4 of the camera. The processor 22 applies a compression algorithm to the digital image signals, and sends the compressed signals to a removable memory card 24 via a connector 26. A representative memory card is a 512 K-byte static random access memory (SRAM) available from Mitsubishi Corp.

Since the compression and related processing ordinarily occurs over several steps, the intermediate products of the processing algorithm are stored in a processing buffer 28. (The processing buffer 28 may also be configured as part of the memory space of the image buffer 18.) The number of image signals needed in the image buffer 18 before digital processing can begin depends on the type of processing, that is, for a block transformation to begin, a block of signals including at least a portion of the image signals comprising a video frame must be available. Consequently, in most circumstances, the compression may commence as soon as the requisite block, e.g., of 16×16 picture elements, is present in the buffer 18.

The input section 2 operates at a rate commensurate with normal operation of the camera while compression, which consumes more time, can be relatively divorced from the input rate. The exposure section 10 exposes the sensor 12 to image light for a time period dependent upon exposure requirements, for example, a time period between 1/1000 second and several seconds. The image charge is then swept from the photosites in the sensor 12, converted to a digital format, and written into the image buffer 18 during a standard rate, which may, for example, correspond to a standard video field or frame rate. The repetition rate of the driving signals provided by the control processor 20 to the sensor 12, the A/D converter 16 and the buffer 18 are accordingly generated to achieve such a transfer. The processing throughput rate of the compression and recording section 4 is determined by the character of an image, i.e., the amount of detail versus redundant information, and the speed of the digital signal processor 22, and may take up to several seconds for an especially complex image.

One desirable consequence of this architecture is that the processing algorithm employed in the compression and recording section may be selected for quality treatment of the image rather than for throughput speed. This, of course, can put a delay between consecutive pictures which may affect the user, depending on the time between photographic events. This is a problem since it is well known and understood in the field of still video recording that a digital still camera should pro-

vide a continuous shooting capability for a successive sequence of images. For this reason, the image buffer **18** shown in FIG. **1** provides for storage of a plurality of images, in effect allowing a series of images to "stack up" at video rates. The size of the buffer is established to hold enough consecutive images to cover most picture-taking situations. FIGS. **2A** and **2B** show the typical functional sequence for a camera having buffer area for three separate images. As each image is captured (line D), the next available buffer area is loaded (line E) and image compression begins (line F). FIG. **2A** illustrates a typical situation in which the shutter release (line C) is actuated at spaced times insufficient to load all three buffer areas. In FIG. **2B**, the shutter release is continuously held down (line C) and a burst of exposures ensue. The three buffer areas are quickly loaded (line E) and, responsive to a buffer full signal (line H), the control processor **20** interrupts the exposure section **10**. No further image is then captured until a buffer is freed. For example, in lines E and F, after the first image is compressed and transferred to the card **24**, the first buffer area is freed up and a fourth exposure is made.

An operation display panel **30** is connected to the control processor **20** for displaying information useful in operation of the camera. Such information might include typical photographic data, such as shutter speed, aperture, exposure bias, color balance (auto, tungsten, fluorescent, daylight), field/frame, low battery, low light, exposure modes (aperture preferred, shutter preferred), and so on. Moreover, other information unique to this type of camera is displayed. For instance, the memory card **24** would ordinarily include a directory signifying the beginning and ending of each stored image. This would show on the display **30** as either (or both) the number of images stored or the number of image spaces remaining, or estimated to be remaining.

The control processor **20** also accesses a card diagnostics memory **31** for generating important information about the condition of the memory card **24**. Specifically, the connector **26** is queried for the presence of a card **24** and, if no card is connected, a "no card" display is produced on the operation display **30**. Likewise, if a card is present but it is full of images, a "card full" display is produced. The card diagnostics memory **31** also provides a verification routine to check the card **24** for faults or defects. For instance, a set of code patterns (such as 010101 . . . and 101010 . . . ) can be written into and read from the card to verify memory locations. This is especially important since compressed data is stored on the card **24** and even one defective memory location can produce an extensive visual artifact in the expanded picture. If a card **24** fails the verification test, a "defective card" display is produced on the operation display **30**.

Buffer diagnostics are maintained in a memory **32** for producing certain information about the condition of the image buffer **18**. Its principal purpose is to monitor the utilization of buffer space and produce, as shown in line H of FIG. **2B**, a "buffer full" signal when no more buffer space is available. A corresponding display is produced on the display **30**, which is important to the user as no further image can be captured until a buffer area is freed up. The digital signal processor **22** further provides a signal indicative of the compression operation on a line **30***a* to the operation display **30**, that is, a signal indicating that compression is underway. A corresponding display, "compression underway", is activated by the display **30**.

The digital signal processor **22** compresses each still video image stored in the image buffer **18** according to a known image compression algorithm shown in FIG. **1B**. The compression algorithm begins with a discrete cosine transformation (block **33**) of each successive block of the image data to generate a corresponding block of cosine transform coefficients. It is well-known that compression techniques are greatly enhanced when applied to image data which has been previously transformed in accordance with a discrete cosine transform algorithm. The cosine transform coefficients are then rearranged in serial order by a block-to-serial conversion step (block **34**) described and illustrated in U.S. Pat. No. 4,772,956, "Dual Block Still Video Compander Processor," issued Sept. 20, 1988 to Roche et al., and which is assigned to the assignee of the present invention and incorporated by reference into the present patent application. The block-to-serial conversion step consists of arranging the discrete cosine transform coefficients in order of increasing spatial frequency, which corresponds to a zig-zag pattern illustrated in the Roche et al patent. The resulting serial string of transform coefficients is then subjected to thresholding, normalization, and quantization (block **36**) and minimum redundancy encoding (block **38**).

Thresholding discards data words of magnitudes less than a threshold number. Normalization entails dividing each data word by a divisor to yield a quotient. Quantization discards the fractional bits in the quotient. Minimum redundancy encoding is a technique well-known in the prior art and employs two complimentary steps, namely amplitude encoding and run length encoding. Amplitude encoding (or "Huffman Encoding") assigns to each of a finite set of possible amplitudes an encoded bit pattern designed to require the smallest number of bits for non-redundant representation. Run length encoding represents any consecutive run of zeros in the data as the smallest non-redundant bit pattern required to count the number of zeros in the run. The set of bit patterns representing each of the possible word amplitudes and the set of bit patterns representing each of the possible zero run lengths may be selected in accordance with the well-known principles and stored in look-up tables for use during the compression process. This compression technique greatly reduces the number of bits required to represent a frame of still video information, without reduction in image quality, thereby greatly reducing the amount of storage that must be allocated to each still frame in the SRAM card **24**.

The uncompressed still video data stored in the image buffer **18** is organized in the manner of a television picture, that is, in vertical columns and horizontal rows of video data bytes (representing the corresponding picture elements) divisible into square blocks of bytes, each block comprising, e.g., 16 columns and 16 rows of bytes. The control processor **20** fetches a block of data each time the digital signal processor **22** is about to execute the compression algorithm. The compression process eliminates many bits contained in each block of video data, so that the compressed video data does not emerge from the processor **22** as a standard-length stream of bits, but as a variable number of bits dependent upon the complexity of the picture and the rules used for truncating bits. The memory space, therefore, allocated for each image in the SRAM card **24** can vary from image to image. The processor **22**, consequently,

allocates memory space in the SRAM card **24** after each compression sequence for an image is completed so that the images may be "packed" into the card as a continuum of compressed image data. This means the storage capacity, in terms of actual images, of the SRAM card is unknown in the beginning, and then gradually is specified as pictures are taken and the card is "filled". The control processor **20** monitors the numbers of images, furnishing a running total to the operation display panel **30**, and further triggers a special "one more picture" display when the remaining memory space is sufficient for a predetermined number of, say one more, pictures. Alternatively, a fixed "maximum" space can be allocated in the SRAM card **24** for each image; in this case, fewer images can be stored although the total capacity is always known.

What has been described to this point applies equally to monochrome or color pictures, except that color pictures require additional processing. For instance, if a multi-spectral color filter array (shown in broken line **40** in FIG. **1A**) overlies the image sensor **12**, the various colors are sorted out and processed differently for each color. This would be accomplished by an additional routine in the digital signal processor **22**. Such color filter array processing would precede the discrete cosine transform block **33** (FIG. **1B**) so that image compression can be done separately on each color and three compressed frames would be stored in the memory card **24** for each image.

FIG. **3** illustrates details of a specific processing architecture in which an image buffer **39** combines the function of the image buffer **18** and the processing buffer **28** shown in FIG. **1A**. The analog signals from the output diode **14** of the image sensor **12** are gamma-corrected in a conventional linear-to-gamma correction circuit **74** and applied to the A/D converter **16**. The output of the A/D converter **16** is connected to an 8 bit-to-32 bit latching array **76** comprising latches **76***a*, **76***b*, **76***c*, and **76***d*. In practice, the latching array **76** performs a double buffering operation to save time, that is, the latched bytes are unloaded in pairs to the processor **22** on a 32 bit-wide input data bus **22***a*, as follows. After latches **76***a* and **76***b* are loaded with the first two bytes provided by the A/D converter **16**, the latched bytes are applied in parallel to the data bus **22***a*. In the meantime other two latches **76***c* and **76***d* are being loaded with the next two bytes. When the latches **76***c* and **76***d* are full, the latched bytes are applied in parallel to the input data bus **22***a* while the other latches **76***a* and **76***b* are being loaded with new bytes.

In this architecture, therefore, the digital signal processor **22** has the initial function, prior to compression, of transferring the paired input bytes to the image buffer **39**, which includes random access memories (RAMs) **78***a*, **78***b*, **78***c*, and **78***d*. In terms of allocating bytes to storage, RAM **78***a* receives data from the latch **76***a*, RAM **78***b* from latch **76***b*, and so on. The digital signal processor **22** produces address words on an address bus **22***c* connected to the RAMs **78***a*–**78***d*. The address word is held in an address latch **80** while a portion of the address word is decoded in a decoder **82** for activating the appropriate chip enable ports of the image buffer RAMs **78***a*–**78***d*. As shown in FIG. **3**, the buffer **39** is enabled in pairs of RAMs **78***a*–**78***d* to correspond to the paired bytes being transferred from the latches **76***a*–**76***d*.

The embodiment of FIG. **3** includes no resident non-volatile memory for the digital processor **22**. Consequently, the operating program code for the camera is stored in a programmable read only memory (PROM) **84** connected to the address and data buses of the control processor **20**. These bus lines are also connected, through respective buffers **86** and **88**, to the output address bus **22***c* and the output data bus **22***d* of the digital processor **22**. The control processor **20** downloads portions of the operating program from the PROM **84** to the image buffer **39** as required for operation of the digital processor **22**. For instance, when a shutter release **73** is depressed and a line **73***a* is activated, the control processor **20** downloads the data acquisition code over the data bus **22***d* to a specified location in the image buffer **39**. The appropriate address words are then applied to the address bus **22***c* by the control processor **20** and the operating code is written into volatile memory in the digital processor **22**. The processor **22** is then ready to latch incoming image bytes into the latch array **76** and transfer paired bytes to the image buffer **39**.

When all the image bytes of a still picture are in the image buffer **39**, the control processor **20** downloads the operating code for the discrete cosine transform from the PROM **84** to a specified unused memory space in the image buffer **39**. The DCT code is written into the volatile memory of the processor **22** and the discrete cosine transformation is performed on blocks of image bytes in the image buffer **39**. After each block is transformed, the transform coefficients are written back into the image buffer **39**. The control processor **20** next downloads the operating code for the block to serial conversion in like manner, the conversion is performed, and the serial string is written back into the buffer. Then the code for thresholding, normalization and quantization is downloaded in similar fashion, the processing done and processed data stored, and the code for minimum redundancy encoding is downloaded and the amplitude and run length encoding is done. With the image data now in its finally compressed form, and instead of writing the compressed data back into the buffer **39** one more time, the compressed data is directly written into the memory card **24**. The above-related technique for storing the operating code in the PROM **84** and downloading sections thereof as needed conserves on the need for fast, and therefore expensive, non-volatile memory dedicated to the processor **22**.

A simplified block diagram is shown in FIG. **4***a* of a still video player for reproducing a picture or for making a hard copy print from the digital image signals stored in compressed format in the memory card **24**. With the card **24** inserted into a connector **100**, the digital signals are accessed and processed in an expander **102**. An expansion algorithm, which is basically the inverse of the compression algorithm of FIG. **1B**, is shown in FIG. **4B** and implemented by the expander **102**. The digital image data is expanded block-by-block and stored in an image buffer **104** as a decompressed image. A conventional thermal printer **106** is connected to the buffer **104** for making a hard copy thermal print from the decompressed image. In addition, the decompressed image signals are converted to analog form by a digital-to-analog (D/A) converter **108** and displayed on a conventional CRT monitor **110**.

The invention has been described in detail with particular reference to a presently preferred embodiment, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

What is claimed is:

1. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information if generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an input rate commensurate with normal operation of the camera;

digital processing means for operating on blocks of stored digital image signals at a processing throughput rate different than said input rate, said digital processing means including means for transforming blocks of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals;

means responsive to said digital processing means for downloading the processed image signals to said removable digital memory; and

diagnostic means for monitoring the utilization of said image buffer whereby information is generated as to the current condition of the image buffer.

2. The apparatus claimed in claim 1 in which said diagnostic means includes means for monitoring the remaining storage capacity of said image buffer.

3. The apparatus as claimed in claim 2 in which said diagnostic means includes means for providing a buffer full signal when said buffer is fully loaded.

4. The apparatus as claimed in claim 3 wherein said control processor means includes means responsive to said buffer full signal for interrupting said exposing means and preventing further exposure of said image sensor.

5. The apparatus as claimed in claim 3 further including a visual indicator and wherein said control processor means activates said visual indicator according to the state of said buffer full signal.

6. The apparatus as claimed in claim 1 in which said digital processing means further includes a processing buffer, said digital processing means operating on blocks of digital image signals before said image buffer is fully loaded and storing intermediate products of said processing in said processing buffer so that memory space is freed in said image buffer for further storage of new still images.

7. The apparatus as claimed in claim 1 which said digital processing means generates in operating signal indicating when the compression algorithm is operating.

8. The apparatus as claimed in claim 7 further including a visual indicator and wherein said control processor means activates said visual indicator according to the state of said operating signal.

9. The apparatus as claimed in claim 1 in which said digital processing means compresses the digital image signal in a plurality of stages, one stage including the performance of a discrete cosine transform on the blocks of image signals and another stage including minimum redundancy encoding of the transformed image signals.

10. An electronic still camera employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said camera including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image signals are obtained from the respective photosites, said camera comprising:

an A/D converter for converting the analog image signals into digital image signals;

a digital processor for processing the digital image signals through a compression algorithm and for generating a stream of compressed signals having a variable bit length dependent upon the character of the image, said processor allocating a variable-length memory space in said removable digital memory for each image;

means for downloading the compressed signals to the allocated image space such that consecutive memory spaces may differ in length depending on the character of each image; and

means for generating a warning signal when the remaining unused memory space in said removable digital memory corresponds to a predetermined amount of memory space generally suitable for at least one more still image.

11. The camera as claimed in claim 10 further including a visual indicator and means for activating said visual indicator according to the state of said warning signal.

12. An electronic still camera employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said camera including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image signals are obtained from the respective photosites, said camera comprising:

an A/D converter for converting the analog image signals into digital image signals;

a random access image buffer having memory space sufficient for a plurality of still images;

control means responsive to repeated actuation of said exposing means for entering the digital image signals corresponding to a sequence of still images into said image buffer at a rate commensurate with normal operation of the camera, said control means intermittently disabling and reenabling said exposing means according to the memory space remaining in said random access image buffer;

a digital processor for compressing the digital image signals, said processor connected to said buffer for operating on stored digital signals from the first stored image irregardless of the entering of digital

signals corresponding to subsequent still images into said buffer; and

means responsive to said digital processor for downloading the compressed image signals to said removable digital memory.

13. The camera as claimed in claim 12 in which said digital processor operates a compression algorithm on blocks of stored digital signals corresponding to blocks of picture elements, said block compression operating irregardless of the entering of digital signals corresponding to further blocks of the same image.

14. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an input rate commensurate with normal operation of the camera;

digital processing means for operating on blocks of stored digital image signals at a processing throughput rate different than said input rate, said digital processing means including means for transforming blocks of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals;

means responsive to said digital processing means for downloading the processed image signals to said removable digital memory; and

diagnostic means for checking the removable digital memory for faults or defects.

15. The apparatus as claimed in claim 14 in which said diagnostic means includes means for providing a defective card signal whenever the removable digital memory fails the check provided by said diagnostic means.

16. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer for storing one or more blocks of digital image signals corresponding to portions of a still image;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer;

digital processing means for operating on each block of stored digital image signals, said digital processing means including means for transforming each block of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals;

diagnostic means for checking the removable digital memory for faults or defects and for providing an indication thereof; and

means responsive to said digital processing means and to said indication from said diagnostic means for downloading the processed image signals to said removable digital memory.

17. The apparatus as claimed in claim 16 in which said diagnostic means includes means for providing a defective card warning signal whenever the removable digital memory fails the check provided by said diagnostic means.

18. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said area image sensor including a color filter array having a multi-colored pattern oriented to said photosites and including one color representative of luminance, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an input rate commensurate with normal operation of the camera;

digital processing means for operating on blocks of stored digital image signals at a processing throughput rate different than said input rate, said digital processing means including means for transforming blocks of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals, said digital processing means interpolating at least the luminance component over the block area and transforming each block of digital signals including the interpolated signals; and

means responsive to said digital processing means for downloading the processed image signals to said removable digital memory.

* * * * *

# Exhibit 5

US005164831A

# United States Patent [19]

Kuchta et al.

[11] Patent Number: 5,164,831

[45] Date of Patent: Nov. 17, 1992

[54] **ELECTRONIC STILL CAMERA PROVIDING MULTI-FORMAT STORAGE OF FULL AND REDUCED RESOLUTION IMAGES**

[75] Inventors: Daniel W. Kuchta, Brockport; Peter J. Sucy, Hamlin, both of N.Y.

[73] Assignee: Eastman Kodak Company, Rochester, N.Y.

[21] Appl. No.: 494,205

[22] Filed: Mar. 15, 1990

[51] Int. Cl.[5] ..... H04N 5/30

[52] U.S. Cl. ..... 358/209; 358/102; 358/909; 358/432; 360/35.1

[58] Field of Search ..... 358/432, 909, 906, 403, 358/433, 445, 447, 448, 452, 458, 133, 459, 209, 471, 102; 360/33.1, 35.1

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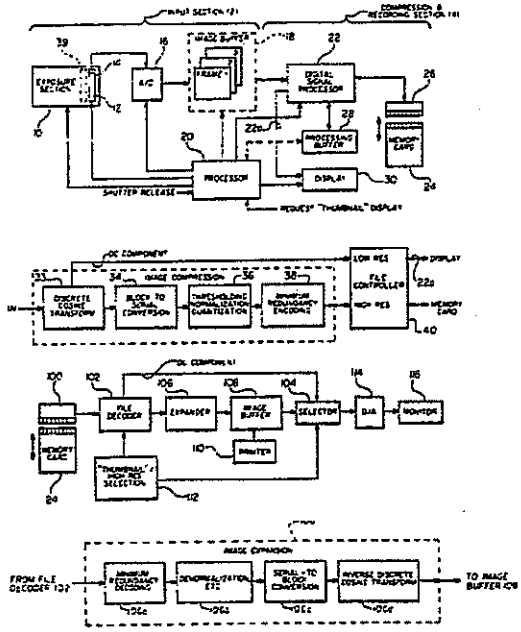
*Primary Examiner*—James J. Groody
*Assistant Examiner*—Jeffrey S. Murrell
*Attorney, Agent, or Firm*—David M. Woods

[57] ABSTRACT

An electronic still camera employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable static random access memory card. An image sensor is exposed to image light and the resultant analog image information is converted to digital image signals. A control processor controls the exposure section and the A/D converter, delivering digital signals to a multi-image buffer at a rate commensurate with normal operation of the camera. A digital processor operates on the stored digital signals, transforming blocks of the digital signals and encoding the signals into a compressed stream of processed image signals, which are downloaded to the memory card. The digital processor operates at a throughput rate different than the input rate for better image capture and optimum utilization of the camera.

15 Claims, 3 Drawing Sheets



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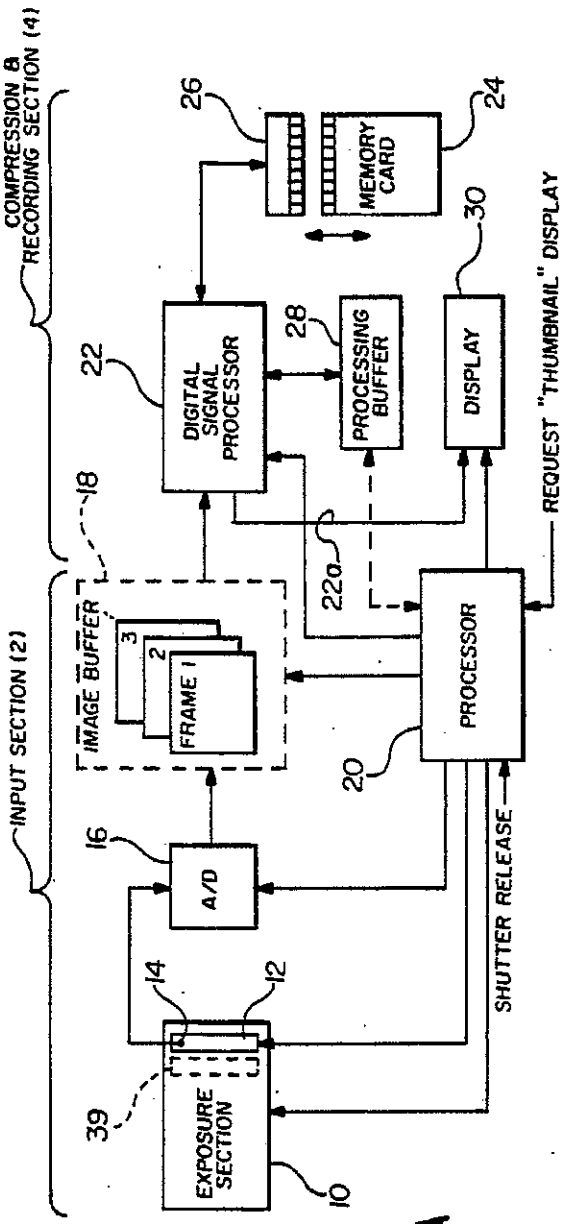
COMPRESSION & RECORDING SECTION (4)
INPUT SECTION (2)
IMAGE BUFFER
FRAME 1
2
3
A/D
EXPOSURE SECTION
DIGITAL SIGNAL PROCESSOR
PROCESSING BUFFER
DISPLAY
MEMORY CARD
PROCESSOR
SHUTTER RELEASE
REQUEST "THUMBNAIL" DISPLAY
10
12
14
16
18
20
22
22a
24
26
28
30
39

FIG. IA

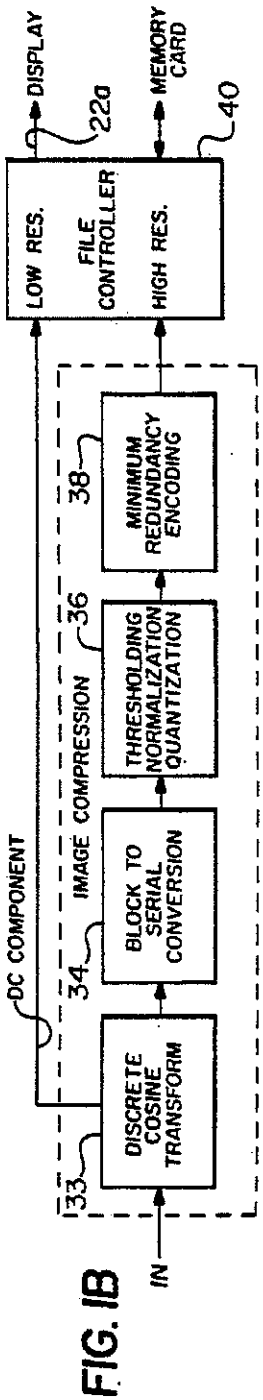
DISPLAY
MEMORY CARD
LOW RES.
FILE CONTROLLER
HIGH RES.
22a
40
DC COMPONENT
IMAGE COMPRESSION
DISCRETE COSINE TRANSFORM
BLOCK TO SERIAL CONVERSION
THRESHOLDING NORMALIZATION QUANTIZATION
MINIMUM REDUNDANCY ENCODING
33
34
36
38
IN

FIG. IB

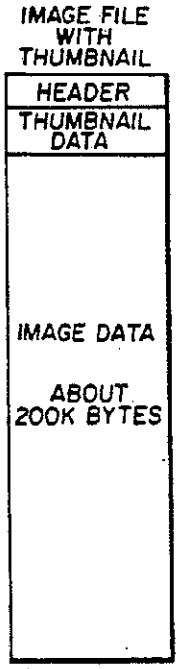
IMAGE FILE WITH THUMBNAIL
HEADER
THUMBNAIL DATA
IMAGE DATA
ABOUT 200K BYTES

FIG. 2A

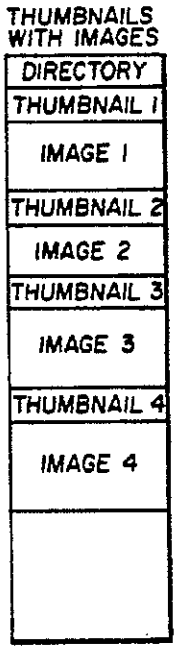
THUMBNAILS WITH IMAGES
DIRECTORY
THUMBNAIL 1
IMAGE 1
THUMBNAIL 2
IMAGE 2
THUMBNAIL 3
IMAGE 3
THUMBNAIL 4
IMAGE 4

FIG. 2B

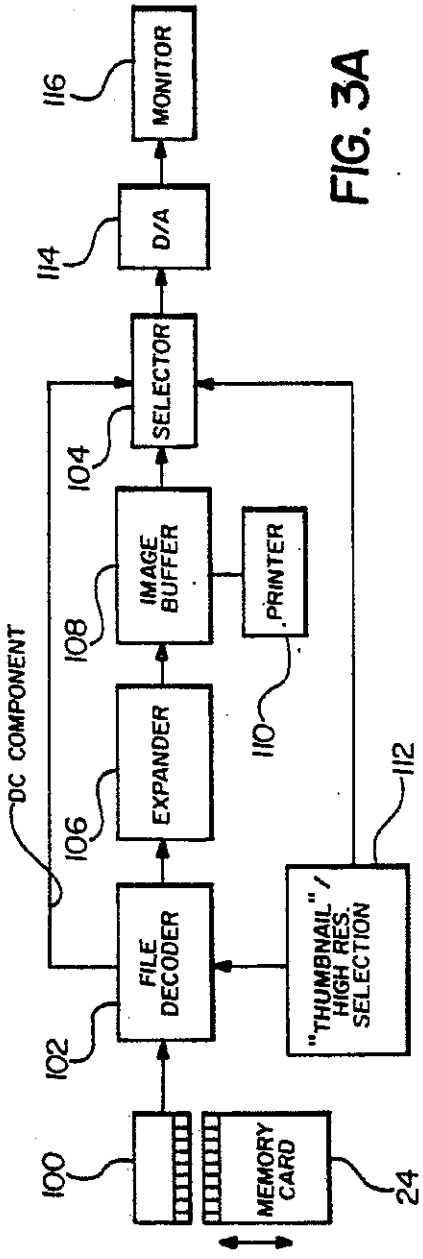


FIG. 3A

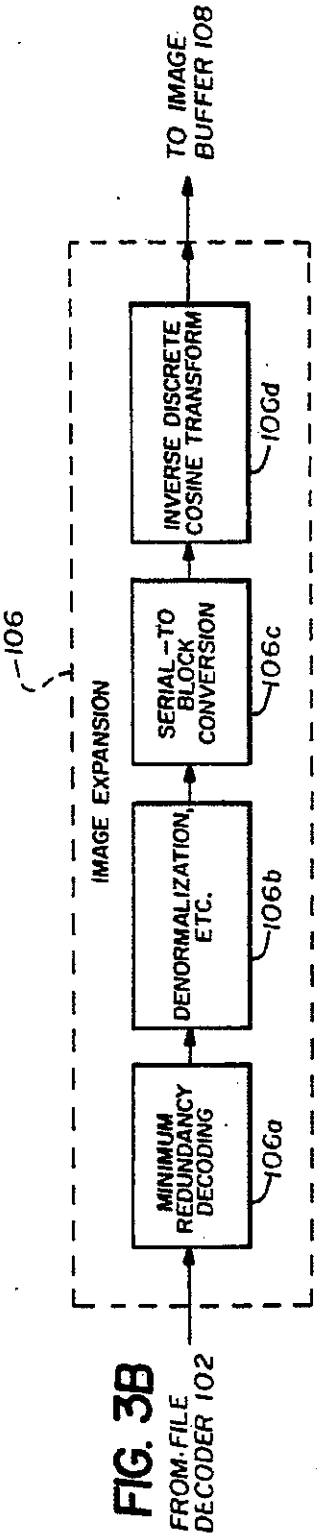


FIG. 3B

AX203277

# ELECTRONIC STILL CAMERA PROVIDING MULTI-FORMAT STORAGE OF FULL AND REDUCED RESOLUTION IMAGES

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains in general to the field of electronic still imaging and, more particularly, to apparatus incorporating digital processing of image signals derived from an electronic image sensor and digital storage of the processed signals.

2. Description Relative to the Prior Art

An electronic still camera employing non-volatile storage of digital image signals is described in copending U.S. patent application Ser. No. 349,566, filed May 9, 1989 now U.S. Pat. No. 5,016,107 dated May 1, 1991, and assigned to the same assignee as the present invention. The electronic still camera disclosed therein employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable static random access memory card. An image sensor is exposed to image light and the resultant analog image information is converted to digital image signals. The digital signals are delivered to a multi-image buffer at a rate commensurate with normal operation of the camera. A digital processor operates on the stored digital signals, transforming blocks of the digital signals and encoding the signals into a compressed stream of processed image signals, which are downloaded to the memory card. The digital processor operates at a throughput rate different than the input rate, thereby allowing more efficient image capture and optimum utilization of the camera.

Despite efficient operation of such a camera and the use of compression to reduce the amount of data, high quality digital image files written in the memory card are nonetheless quite large and take significant amounts of time to process due to image size, image resolution, and the nature of the compression process. For example, a 1,280 by 1,024 pixel, 24-bit per pixel image might compress over many seconds to 100 to 300 Kilobytes of storage area. It is often desirable to quickly review the images on the memory card before deciding to transmit, to make a copy, or to retake a picture. The physical time for decompression and display of a high resolution image can be so slow as to interfere with the review process.

The matter of electronic preview has been taken up in a number of prior art disclosures. For instance, in U.S. Pat. No. 4,827,347 an electronic still camera includes a Plurality (twelve) of small displays connected to a like plurality of display/framestores so that pictures can be previewed as a group and then individually retained or discarded. The aforementioned processing time problem, however, is not addressed. In U.S. Pat. No. 4,763,208, an electronic still camera cooperates with playback apparatus that subsamples images recorded on a disk and simultaneously displays the subsampled images as a group on a monitor. While with this construction the contents of the disk can be searched within a shorter time, the subsampled images are unavailable for subsequent review. Research Disclosure item 28618 (p. 71 of the February, 1988 issue) describes a concept for storing video signals from electronically scanned negatives on individual tracks of a video disk while simultaneously storing miniature versions of these pictures in a mosaic frame store. After all the images are recorded on their individual tracks, and the mosaic frame store is accordingly filled, the mosaic-like content of the frame store is itself recorded as a full NTSC frame on a separate track. A similar concept is applied to an all-video picture processing system in U.S. Pat. No. 4,802,019 for rearranging, replacing, or inserting video programs in a sequence of such programs. Each program is characterized by a single frame that is reduced or "squeezed" to one sixteenth its original size and included in a mosaic of like pictures on an index screen. Rearrangement, etc. of the video programs is then made by reference to the index screen. In the latter two systems, the miniaturized pictures are stored together as a video frame. This is of little aid in an all-electronic system in which the pictures are, for example, separately transmitted to a remote location, separately edited, or otherwise used in a way in which continued, rapid review of a particular recorded picture is desirable.



## SUMMARY OF THE INVENTION

The invention is based on the addition of a reduced resolution image to the digital file format for an individual high resolution image. Particularly if the reduced resolution, or "thumbnail", image is created as a part of the image acquisition process, or in close timing thereto, it is convenient to provide multi-format storage of the "thumbnail" image in a reserved area associated with each image file. The "thumbnail" image then follows the high resolution image wherever the image file travels. Since the "thumbnail" image is easily and quickly accessed, reviewing and display is extremely fast.

In accordance with the invention, electronic still imaging apparatus employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory. The imaging apparatus also includes an image sensor having an array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites. The analog image information is converted into digital image signals and, further, reduced resolution signals are generated from the digital image signals. A multi-format image file is formed by combining the (full resolution) digital image signals and the reduced resolution signals. The image file is then stored in the digital memory, where the reduced resolution signals may be quickly accessed for rapid display.

In accordance with a further embodiment of the invention, electronic still image processing apparatus includes an image buffer with storage capacity for storing digital image signals corresponding to a still image. A digital processor transforms blocks of the stored digital image signals into corresponding sets of transform coefficient signals and encodes the coefficient signals into a compressed stream of processed image signals. In addition, the digital processor generates reduced resolution image signals from the stored digital image signals and downloads both the processed (high resolution) image signals and the reduced resolution image signals to a digital memory. In a preferred implementation, the reduced resolution signals are based on the average or dc component coefficient signals generated during the transformation.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, in which:

FIG. 1A is a block diagram of an electronic still camera employing digital processing and multi-format storage according to the invention;

FIG. 1B is a block diagram of an exemplary form of image compression used in connection with the invention;

FIG. 2A is a diagram of a preferred file format for a single full resolution image and its associated "thumbnail" image;

FIG. 2B is a diagram of a preferred file format for several full resolution images and their associated "thumbnail" images;

FIG. 3A is a block diagram of an electronic still player for use in reproducing pictures taken with the camera of FIG. 1A; and

FIG. 3B is a block diagram of an exemplary form of image expansion used in connection with the player of FIG. 3A.

## DETAILED DESCRIPTION OF THE INVENTION

Because electronic still cameras employing charge-coupled device (CCD) sensors are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIGS. 1A and 1B, an electronic still camera is divided generally into an input section 2 and a compression and recording section 4. The input section 2 includes an exposure section 10 for directing image light from a subject (not shown) toward an image sensor 12. Although not shown, the exposure section 10 includes conventional optics for directing the image light through a diaphragm, which regulates the optical aperture, and a shutter, which regulates exposure time. The sensor 12, which includes a two-dimensional array of photosites providing a predetermined picture resolution corresponding to the number of picture elements of the image, is a conventional charge-coupled device (CCD) using either well-known interline transfer or frame transfer techniques. Preferably, the sensor 12 is a high resolution device such as the model KAF-1400 sensor, a 1320(H)×1035(V)-element full-frame CCD imager manufactured by the Eastman Kodak Company. The sensor 12 is exposed to image light so that analog image charge information is generated in respective photosites. The charge information is applied to an output diode 14, which converts the charge information to analog image signals corresponding to respective picture elements. The analog image signals are applied to an A/D converter 16, which generates a digital image signal from the analog input signal for each picture element.

The digital signals are applied to an image buffer 18, which is a random access memory (RAM) with storage capacity for a plurality of still images. A control processor 20 generally controls the input section 2 of the camera by initiating and controlling exposure (by operation of the diaphragm and shutter (not shown) in the exposure section 10), by generating the horizontal and vertical clocks needed for driving the sensor 12, and for clocking image information therefrom, and by enabling the A/D converter 16 in conjunction with the image buffer 18 for each analog signal segment relating to a picture element. (The control Processor 20 would ordinarily include a microprocessor coupled with a system timing circuit.) Once a certain number of digital image signals have been accumulated in the image buffer 18, the stored signals are applied to a digital signal processor 22, which controls the compression and recording section of the camera. The processor 22 applies a compression algorithm to the digital image signals, and sends the compressed signals to a removable memory card 24 via a connector 26. A representative memory card is a 512 K-byte static random access memory (SRAM) available from Mitsubishi Corp. (A 1 megabyte memory card has been recently announced by ITT Canon.)

Since the compression and related processing ordinarily occurs over several steps, the intermediate products of the processing algorithm are stored in a processing buffer 28. (The processing buffer 28 may also be configured as part of the memory space of the image buffer 18.) The number of image signals needed in the image buffer 18 before digital processing can begin depends on the type of processing, that is, for a block transformation to begin, a block of signals including at least a portion of the image signals comprising a video frame must be available. Consequently, in most circumstances, the compression may commence as soon as the requisite block, e.g., of 16×16 picture elements, is present in the buffer 18.

The input section 2 operates at a rate commensurate with normal operation of the camera while compression, which consumes more time, can be relatively divorced from the input rate. The exposure section 10 exposes the sensor 12 to image light for a time period dependent upon exposure requirements, for example, a time period between 1/1,000 second and several seconds. The image charge is then swept from the photosites in the sensor 12, converted to a digital format, and written into the image buffer 18 during a standard rate, which may, for example, corresPond to a standard video field or frame rate. The repetition rate of the driving signals provided by the control processor 20 to the sensor 12, the A/D converter 16 and the buffer 18 are accordingly generated to achieve such a transfer. The processing throughput rate of the compression and recording section 4 is determined by the character of an image, i.e., the amount of detail versus redundant information, and the speed of the digital signal processor 22, and may take up to several seconds for an especially complex image. For this reason, the image buffer 18 shown in FIG. 1 provides for storage of a plurality of images, in effect allowing a series of images to "stack up" at video rates. Further description of the operation of the image buffer is provided in the aforementioned, copending U.S. patent application Ser. No. 349,566.

In addition to the full resolution, compressed image, the digital signal processor 22 generates a reduced resolution, or "thumbnail", image from the original image and outputs the reduced resolution image, together with the compressed image to the memory card 24 as a multi-format image file. A multi-format image file with a "thumbnail" area as it would appear on the memory card 24 is shown in FIG. 2A for one image and in FIG. 2B for several images. In each case, the reduced resolution image signals occupy a defined area near the beginning of each image file. A header may be used before each image file (FIG. 2A) or a directory can identify the location of each image file (FIG. 2B) on the card. On request from the processor 20, the digital signal processor 22 recovers the "thumbnail" image from the image file and outputs it on a line 22a to a display device 30.

Inasmuch as the "thumbnail" image is itself low resolution, the display device 30 may be a low resolution electro-optical device such as a liquid-crystal display. Alternatively, the display device 30 can be of higher resolution and display the "thumbnail" image in a window or portion of the display space.

The "thumbnail" image may be generated by any one of several methods. Average values could be determined for given areas of the original image, or the original image could be subsampled over its entire area. The resulting "thumbnail" data could be grey-scale or full color, and the number of bits/per pixel could vary to suit the needs of the application. In any case, the criteria would be that 1) the "thumbnail" data should add a minimum amount to the overall file size and 2) the "thumbnail" image should contain enough information to present a recognizable representation of the original image.

The digital signal processor 22 compresses each still video image stored in the image buffer 18 according to the image compression algorithm shown in FIG. 1B. The compression algorithm begins with a discrete cosine transformation (block 33) of each successive block of the image data to generate a corresponding block of cosine transform coefficients. It is well-known that compression techniques are greatly enhanced when applied to image data which has been previously transformed in accordance with a discrete cosine transform algorithm. The "thumbnail" image data is preferably taken from the discrete cosine transformation (as will be explained) and applied to a file controller (block 40), which provides the "thumbnail" data on the line 22*a* to the display device 30 and combines the compressed data with the "thumbnail" data to provide the multi-format image file to the memory card 24.

The cosine transform coefficients are rearranged in serial order by a block-to-serial conversion step (block 34) described and illustrated in U.S. Pat. No. 4,772,956, "Dual Block Still Video Compander Processor," issued Sep. 20, 1988 to Roche et al, and which is assigned to the assignee of the present invention and incorporated by reference into the present patent application. The block-to-serial conversion step consists of arranging the discrete cosine transform coefficients in order of increasing spatial frequency, which corresponds to a zig-zag pattern illustrated in the Roche et al patent. The resulting serial string of transform coefficients is then subjected to conventional thresholding, normalization, and quantization (block 36) and minimum redundancy encoding (block 38). Thresholding discards data words of magnitudes less than a threshold number. Normalization entails dividing each data word by a divisor to yield a quotient. Quantization discards the fractional bits in the quotient. Minimum redundancy encoding is a technique well-known in the prior art for reducing the number of bits required to represent a frame of video information, without reduction in image quality, thereby greatly reducing the amount of storage that must be allocated to each still frame in the memory card 24.

The compressed video data does not emerge from the processor 22 as a standard-length stream of bits, but as a variable number of bits dependent upon the complexity of the picture and the rules used for truncating bits. The memory space, therefore, allocated for each image in the memory card 24 can vary from image to image. The processor 22, consequently, allocates memory space in the memory card 24 after each compression sequence for an image is completed so that the multi-format image files may be "packed" into the card as a continuum of compressed image data. This means the storage capacity, in terms of actual images, of the memory card is unknown in the beginning, and then gradually is specified as pictures are taken and the card is "filled". Alternatively, a fixed "maximum" space can be allocated in the memory card 24 for each multi-format image file; in this case, fewer images can be stored although the total capacity is always known.

What has been described to this point applies equally to monochrome or color pictures, except that color pictures require additional processing. For instance, if a multi-spectral color filter array (shown in broken line 39 in FIG. 1A) overlies the image sensor 12, the various colors are sorted out and processed differently for each color. This would be accomplished by an additional routine in the digital signal processor 22. Such color filter array processing would precede the discrete cosine transform block 33 (FIG. 1B) so that image compression can be done separately on each color and three compressed frames would be stored in the memory card 24 for each image.

Despite the degree of compression, a high quality digital image derived from a high resolution sensor can be large and, due to the necessity of decompression or expansion, require significant amounts of time to display due to size, resolution, and compression schemes. In keeping with the invention, the "thumbnail" or reduced resolution image is added to the compressed digital file format to make reviewing the image at any point in the imaging chain very fast. In terms of the multi-format file, a "thumbnail" image is a much smaller data file added to the original image data file. Although the image file may vary in length due to compression techniques, the "thumbnail" image would always be a known size based on the number of pixels in the original image.

An example would be a 1,280 by 1,024 pixel, 24-bit per pixel, compressed original image stored on a RAM-card mass storage device. This file might take on the order of 100 to 300 kilobytes of storage area depending on compression type. To display the image, it must first be expanded, and the resulting 4 Megabytes of information transferred to a display device. A "thumbnail" image is constructed by using the average value of each 16 by 16 pixel area in the original image to represent each pixel of the "thumbnail" image. If each pixel has an 8-bit grey scale, this would add about 5 Kilobytes to the overall image file size. To display the "thumbnail" image, no expansion is necessary, and only 5 Kilobytes of information needs to be transferred to the display device. The resulting image would be of sufficient quality to identify the subject matter of the original.

A "thumbnail" image generated from average values is preferable to one generated by simple subsampling (throwing away all but one pixel in a block). The averaged image looks more like the original with much less "blockiness" and less loss of detail. The preferred method for generating the "thumbnail" images uses the average or dc values from the DCT (Discrete Cosine Transform) algorithm, which were generated for compression of the image. The DCT algorithm produces one dc value for each block of the image being compressed. The dc value is a set of red, green, and blue values which are the mathematical average of the red, green and blue planes of pixels in the block. Alternatively, the mathematical average can be calculated outright over a block of pixels. This is done by actually

summing all the red values and dividing by the number of pixels to create an average red value, and then repeating for the green and blue planes.

A simplified block diagram is shown in FIG. 3A of a still video player for reproducing a picture or for making a hard copy print from the digital image signals stored in compressed format in the memory card **24**. With the card **24** inserted into a connector **100**, the digital signals are accessed and processed in the decoder **102**. The stored dc component of the transform (the "thumbnail" data) is directly applied to a selector **104** while the compressed image data is applied to an expander **106**. An expansion algorithm, which is the conventional inverse of the compression algorithm of FIG. 1B, is shown in FIG. 3B and implemented by the expander **106** which includes a conventional sequence of minimum redundancy decoding (block **106***a*), denormalization (block **106***b*), serial-to-block conversion (block **106***c*), and inverse discrete cosine transformation (block **106***d*). The digital image data is expanded block-by-block and stored in an image buffer **108** as a decompressed image. A conventional thermal printer **110** is connected to the buffer **108** for making a hard copy thermal print from the decompressed image. The output of the image buffer **108** is also connected to the selector **104**, which is under control of an operator-designated selection routine **112**. When a "thumbnail" image is to be observed, the selector **104** routes the "thumbnail" data through a digital-to-analog (D/A) converter **114** to a conventional CRT monitor **116**. Alternatively, the decompressed image signals are converted to analog form by the digital-to-analog (D/A) converter **114** and displayed on the conventional CRT monitor **116**.

A principal advantage of the file format shown in FIGS. 2A and 2B is that an image, with its associated "thumbnail" representation, can be easily separated from the collection of images on the memory card **24** and transmitted to external devices for further processing. For instance, the image file can be sent to the printer **110** and the "thumbnail" image can be quickly examined on the monitor **116** before committing to a print. Likewise, an image file can be easily downloaded to a transceiving device (not shown) and the "thumbnail" image can be examined before deciding to transmit. If the entire image file is transmitted, the "thumbnail" image can be quickly recovered at the receiving end for a preview of the final image. Moreover, for a plural number of images, the corresponding "thumbnail" images can be quickly accessed and displayed either in a mosaic frame or in sequence in order to select the desired full resolution image for printing, displaying, transmitting, etc. Furthermore, the "thumbnail" images can be played back by a dedicated player such as illustrated in FIG. 3A or by a personal computer or like device that is programmed to accomplish the functions outlined in FIG. 3A. In the latter case, the personal computer forms the interface between the memory card **24** and a printer, a monitor, a transceiver, etc.

The invention has been described in detail with particular reference to a presently preferred embodiment, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

What is claimed is:

**1**. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an image sensor having an array of photosites corresponding to picture elements of the still image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to a predetermined picture resolution;

means for subsampling said digital image signals to generate reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution;

means for generating a multi-format image file representative of plural resolutions of the still image from the combination of said digital image signals and said reduced resolution image signals, said combination forming a singular file structure in which said reduced resolution image signals occupy a defined file area in relation to said digital image signals and are commonly accessible therewith for display and processing; and

means for storing the image file in said digital memory.

**2**. The apparatus as claimed in claim **1** further including:

display means for generating a display image;

means for selecting an image file stored in said digital memory; and

means for applying said reduced resolution image signals from said stored image file to said display means to generate a low resolution display of the still image.

**3**. The apparatus as claimed in claim **1** in which the sensor is sequentially exposed to a plurality of still images, said digital image signals and said reduced resolution image signals therefore corresponding to said plurality of images, said file generating means generating a separate multi-format image file for each still image from the digital image signals and the reduced resolution signals corresponding thereto, and said storing means storing each multi-format image file in said digital memory.

**4**. Electronic still imaging apparatus employing digital processing of image signals acquired from a plurality of still images and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of an image and means for exposing said sensor to image light so that analog image information is generated in respective photosites for each acquired image, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to respective picture elements;

an image buffer for storing digital image signals corresponding to blocks of picture elements;

digital processing means for transforming blocks of stored digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a stream of compressed signals;

means responsive to said stored digital image signals for generating reduced resolution image signals corresponding to a reduced resolution version of each image;

means for forming a multi-format image file representative of plural versions of each acquired image,

each image file including the reduced resolution image signals and the compressed signals for a particular still image; and

means for downloading said image file for each acquired image to said removable digital memory.

5. The apparatus as claimed in claim 4 in which the reduced resolution image signals are generated from an average value of the digital image signals corresponding to each block of picture elements.

6. The apparatus as claimed in claim 5 in which the average values of the digital image signals are derived from the transform coefficient signals.

7. Electronic image processing apparatus employing digital processing of image signals corresponding to picture elements of a still image and storage of the processed image signals in a digital memory, said image processing apparatus comprising:

an image buffer for storing digital image signals corresponding to blocks of picture elements;

digital processing means for transforming blocks of stored digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a stream of compressed image signals, said digital processing means further generating reduced resolution image signals from said stored digital image signals;

means for generating a multi-format image file representative of plural resolutions of the still image, said image file including the reduced resolution image signals and the compressed image signals; and

means responsive to said digital processing means for downloading the image file to said digital memory.

8. Apparatus as claimed in claim 7 in which said digital processing means generates an average signal for each block of stored digital image signals and said reduced resolution image signals are formed from said average signals.

9. An electronic image processing system employing digital processing of image signals corresponding to picture elements of a still image and storage of the processed image signals in a digital memory, said image processing system comprising:

an image buffer for storing digital image signals corresponding to blocks of picture elements;

digital processing means for transforming blocks of stored digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a stream of compressed image signals, said digital processing means further generating reduced resolution image signals from said stored digital image signals;

means for generating a multi-format image file representative of plural resolutions of the still image, said image file including the reduced resolution image signals and the compressed image signals;

means responsive to said digital processing means for downloading the image file to said digital memory;

means for selecting an image file stored in said digital memory; and

playback means for operating on the selected image file and generating a reduced resolution image display from said reduced resolution image signals.

10. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an image sensor having an array of photosites corresponding to picture elements of the still image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to a predetermined picture resolution;

means for averaging said digital image signals over local areas of the still image to generate reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution;

means for generating a multi-format image file representative of plural resolutions of the still image from the combination of said digital image signals and said reduced resolution image signals, said combination forming a singular file structure in which said reduced resolution image signals occupy a defined file area in relation to said digital image signals and are commonly accessible therewith for display and processing; and

means for storing the image file in said digital memory.

11. The apparatus as claimed in claim 10 further including:

display means for generating a display image;

means for selecting an image file stored in said digital memory; and

means for applying said reduced resolution image signals from said stored image file to said display means to generate a low resolution display of the still image.

12. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an image sensor having an array of photosites corresponding to picture elements of the still image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to a predetermined picture resolution;

means operating on blocks of digital image signals for compressing said digital image signals and generating averages over said blocks;

means responsive to said averages produced by said compressing means for generating reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution;

means for generating a multi-format image file representative of plural resolutions of the still image from the combination of said compressed digital image signals and said reduced resolution image signals, said combination forming a singular file structure in which said reduced resolution image signals occupy a defined file area in relation to said compressed digital image signals and are commonly accessible therewith for display and processing; and

means for storing the image file in said digital memory.

13. The apparatus as claimed in claim 12 in which said compressing means compresses the digital image signals in a plurality of stages, one stage including the performance of a discrete cosine transform on blocks of digital

image signals and another stage including minimum redundancy encoding of the transformed image signals.

**14.** The apparatus as claimed in claim **13** wherein said discrete cosine transform produces a dc component and said reduced resolution image signals are generated from the dc component of the discrete cosine transform.

**15.** The apparatus as claimed in claim **12** further including:



display means for generating a display image;

means for selecting an image file stored in said digital memory; and

means for applying said reduced resolution image signals from said stored image file to said display means to generate a low resolution display of the still image.

* * * * *

# Exhibit 6

US005440343A

# United States Patent [19]

Parulski et al.

[11] Patent Number: 5,440,343

[45] Date of Patent: Aug. 8, 1995

[54] MOTION/STILL ELECTRONIC IMAGE SENSING APPARATUS

[75] Inventors: Kenneth A. Parulski; Eric G. Stevens, both of Rochester; Robert H. Hibbard, Fairport, all of N.Y.

[73] Assignee: Eastman Kodak Company, Rochester, N.Y.

[21] Appl. No.: 203,237

[22] Filed: Feb. 28, 1994

[51] Int. Cl.[6] ..... H04N 5/335

[52] U.S. Cl. ..... 348/316; 348/322; 348/220

[58] Field of Search ..... 348/207, 220, 294, 316, 348/317, 311, 314, 315, 322, 323, 297; H04N 5/335

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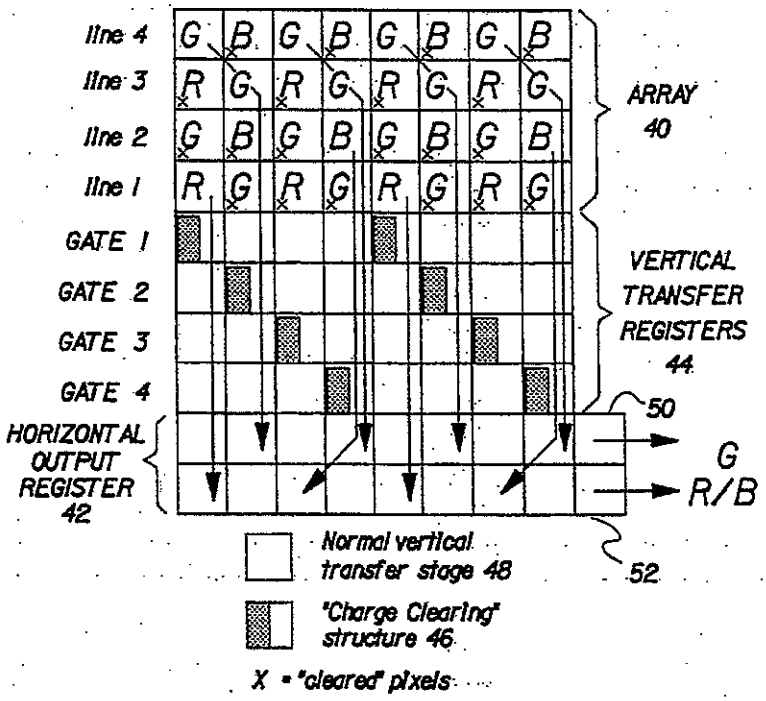
*Primary Examiner*—Michael T. Razavi
*Assistant Examiner*—Tuan V. Ho
*Attorney, Agent, or Firm*—David M. Woods

[57] ABSTRACT

An electronic imaging system is provided that records both motion and still video images. In a motion mode of operation, the electronic imaging system records NTSC resolution images at a standard thirty frame per second rate. In a still mode of operation, the electronic imaging system records megapixel resolution still images at a much lower frame rate. The electronic imaging system utilizes an electronic image sensor that incorporates column selective "charge clearing" structures and column selective "charge parking" structures. The charge clearing structures are used to selectively discard the signal charge from certain color pixels. The charge parking structures are used to sum the charge from multiple vertical pixels. The architecture of the electronic image sensor also allows different image aspect ratios to be provided for the motion and still modes described above.

12 Claims, 10 Drawing Sheets




AXD024517

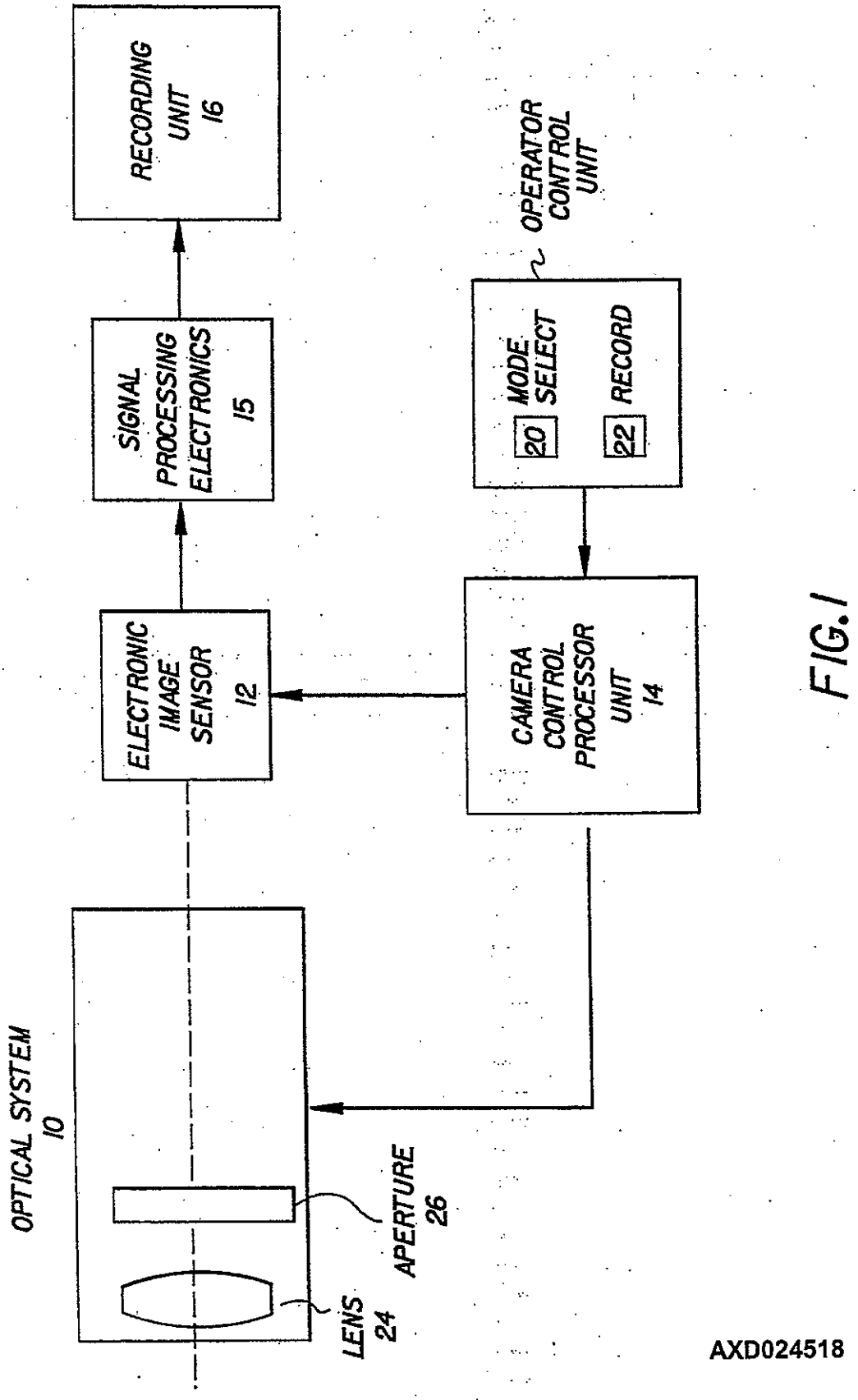

RECORDING UNIT 16
SIGNAL PROCESSING ELECTRONICS 15
ELECTRONIC IMAGE SENSOR 12
OPTICAL SYSTEM 10
LENS 24
APERTURE 26
OPERATOR CONTROL UNIT
MODE SELECT 20
RECORD 22
CAMERA CONTROL PROCESSOR UNIT 14
AXD024518

FIG. 1

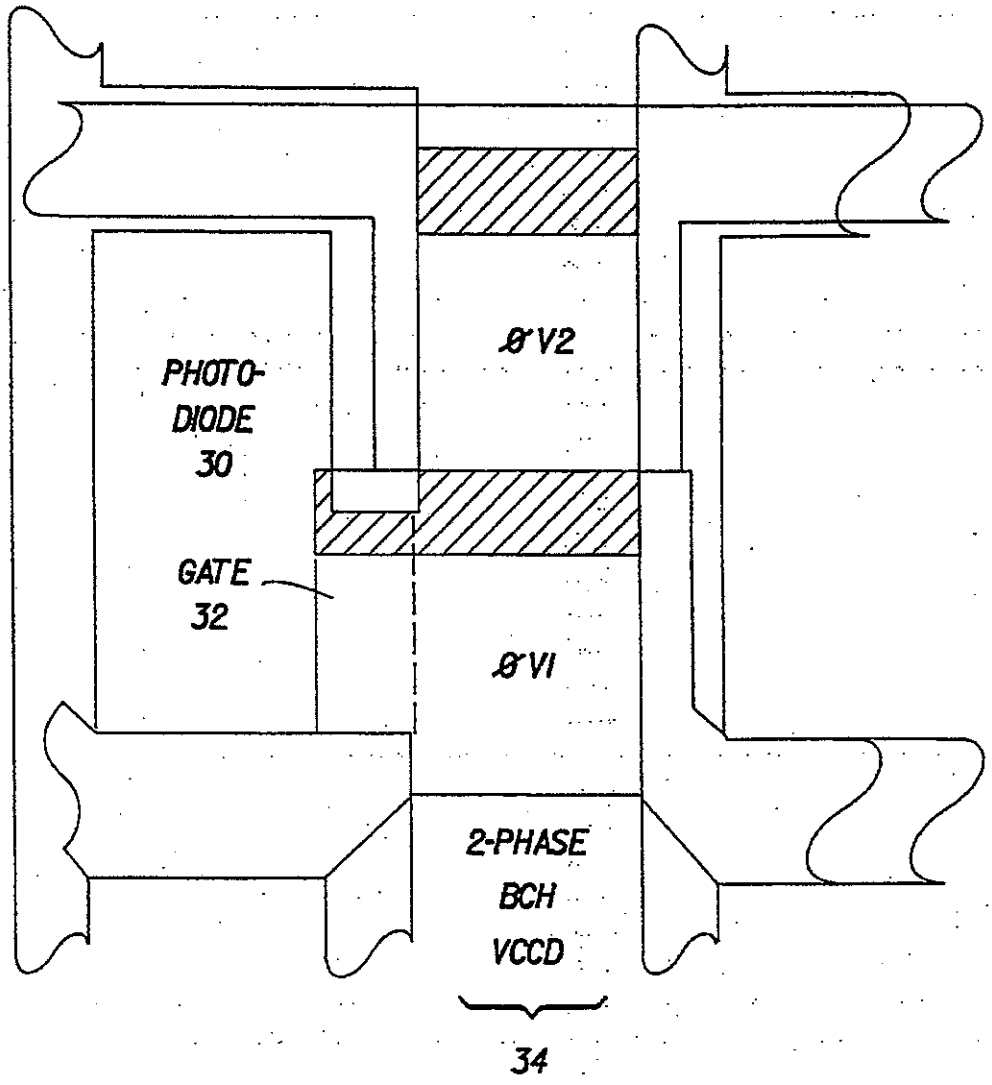



FIG. 2

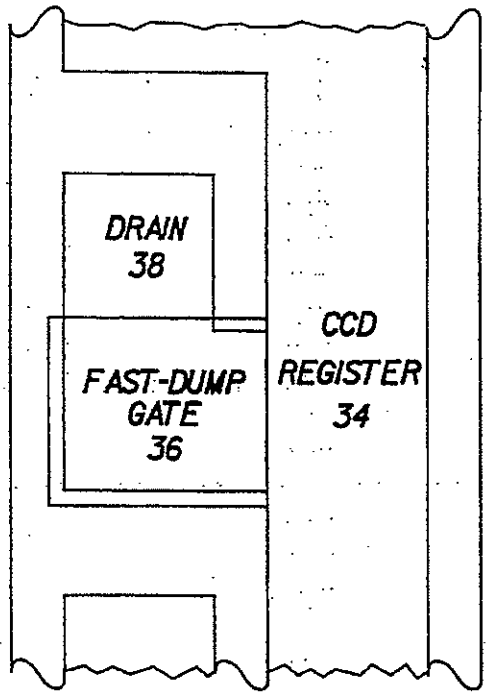



FIG. 3

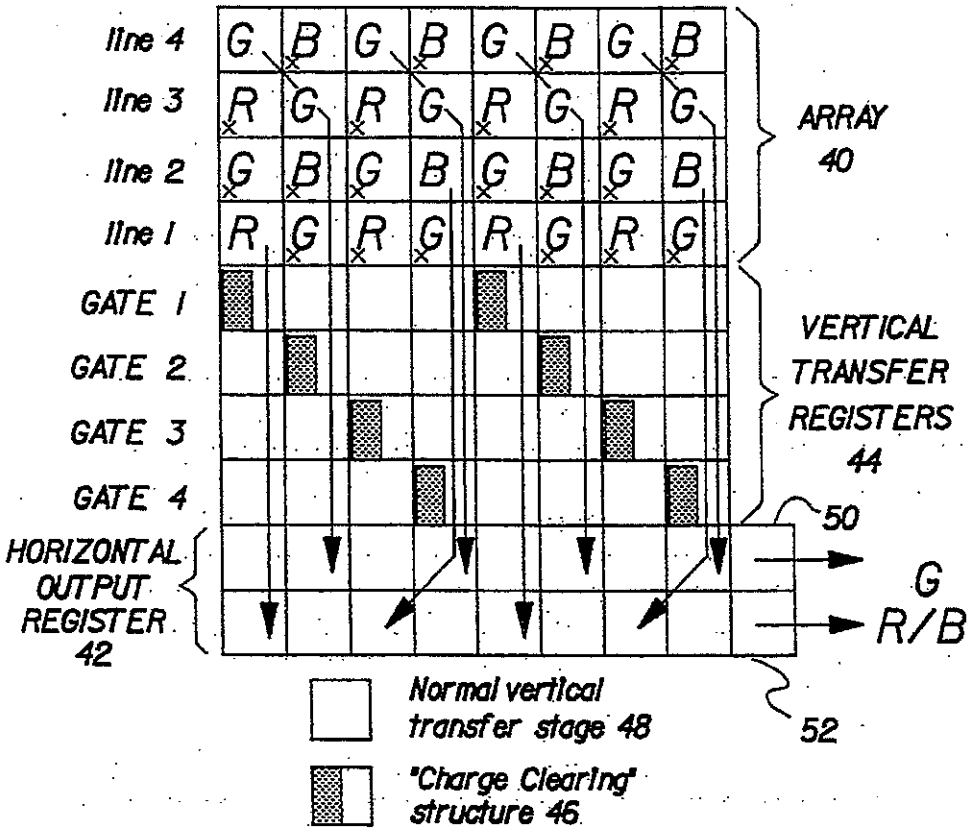



FIG. 4

X = "cleared" pixels

AXD024520

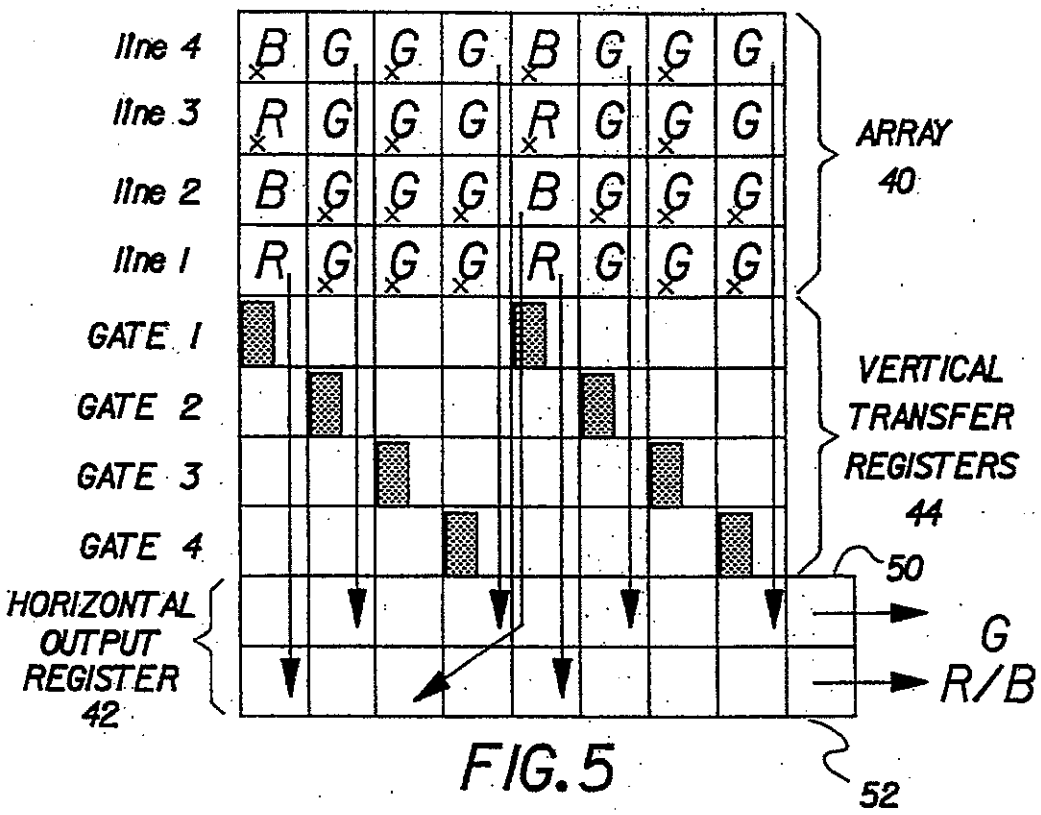



FIG. 5

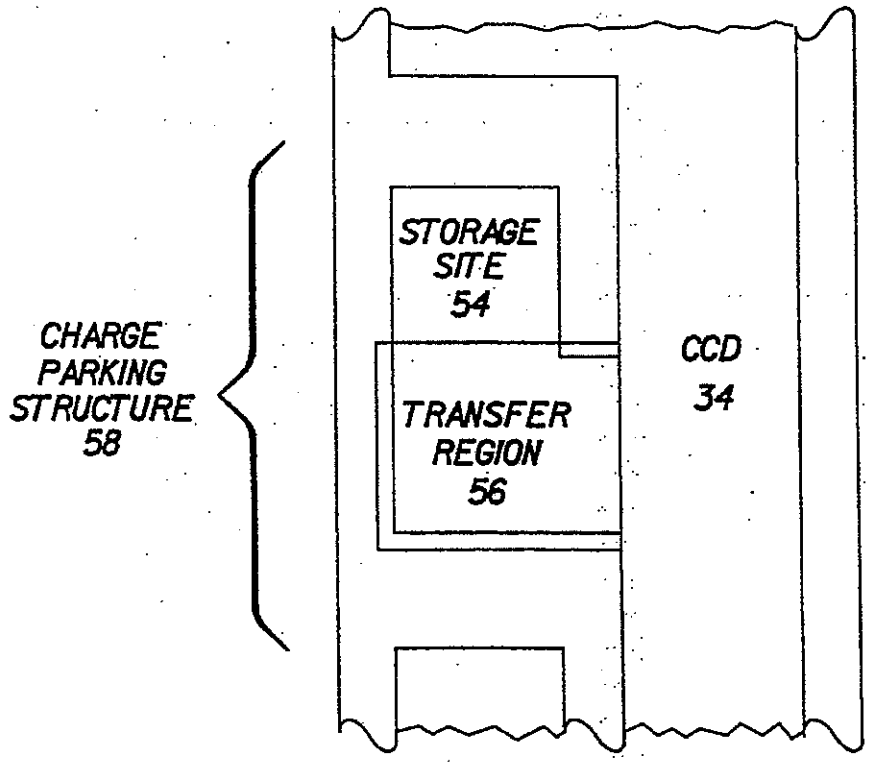



FIG. 6

AXD024521

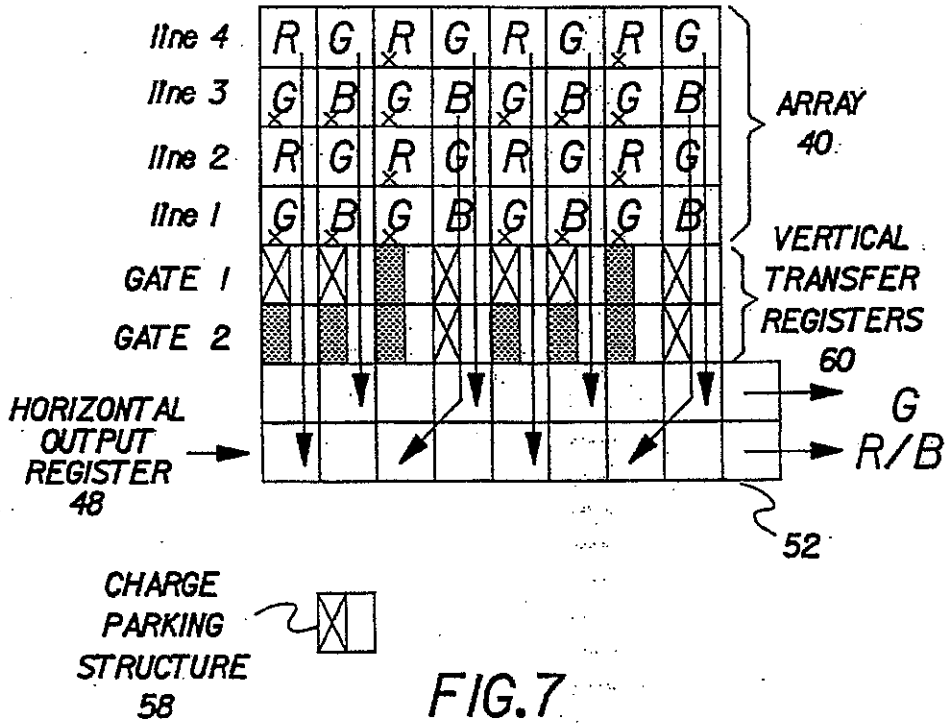



FIG.7

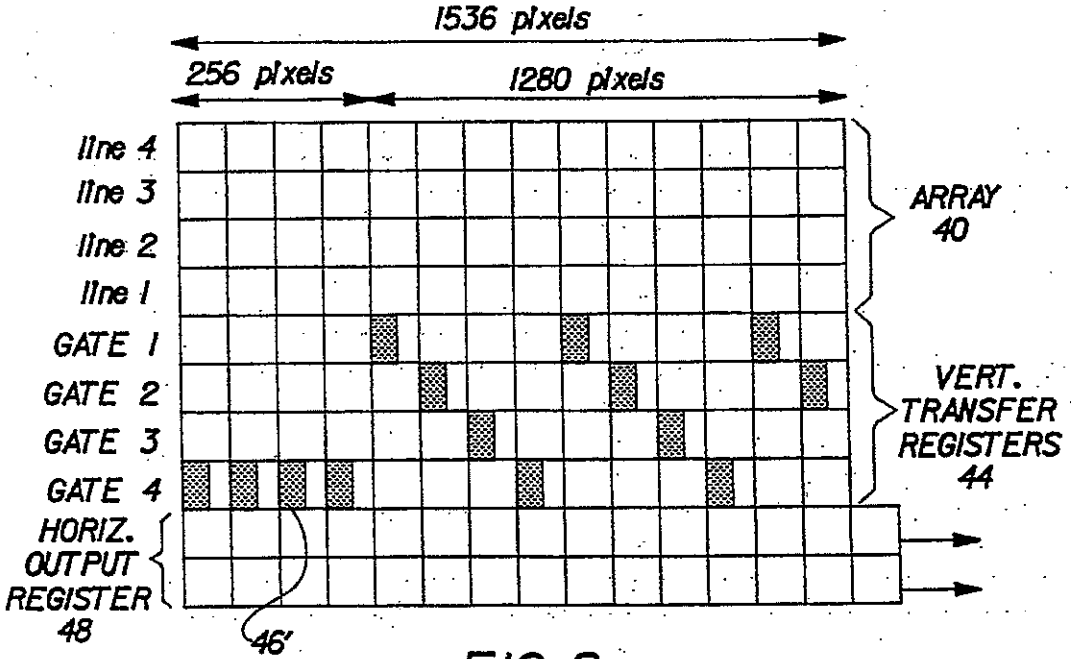



FIG.8

AXD024522

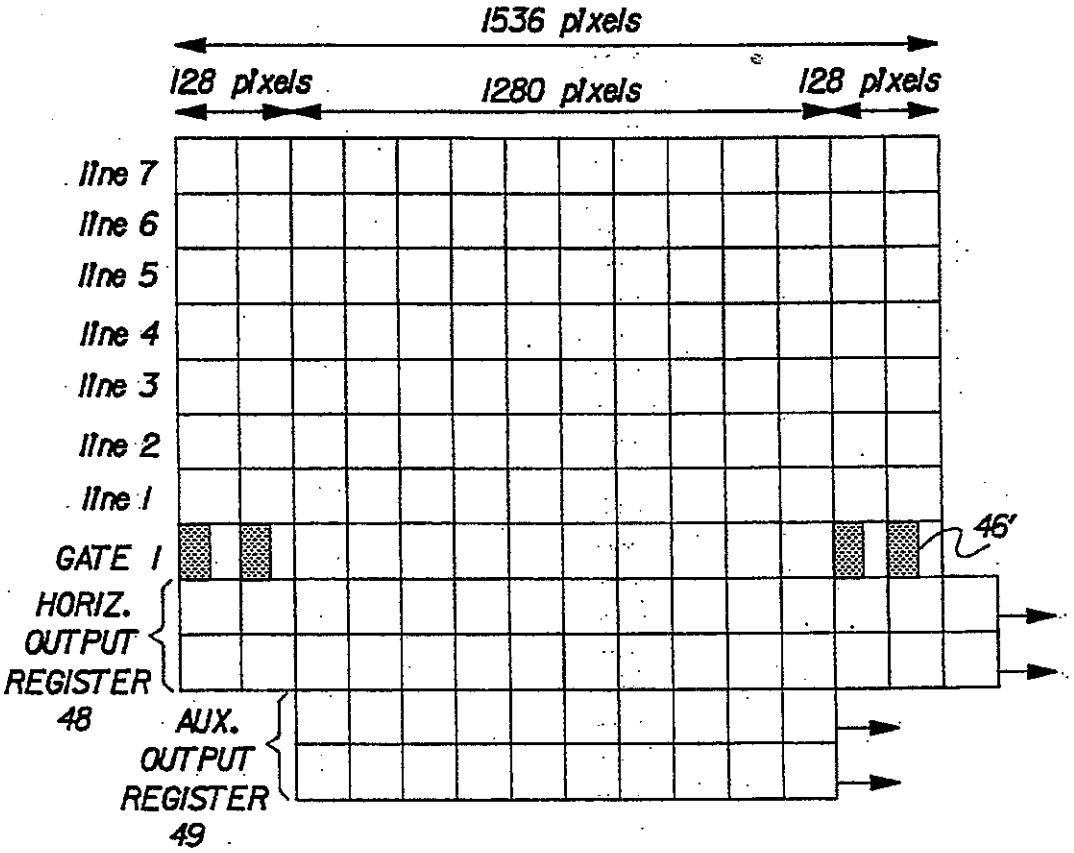



FIG. 9

AXD024523

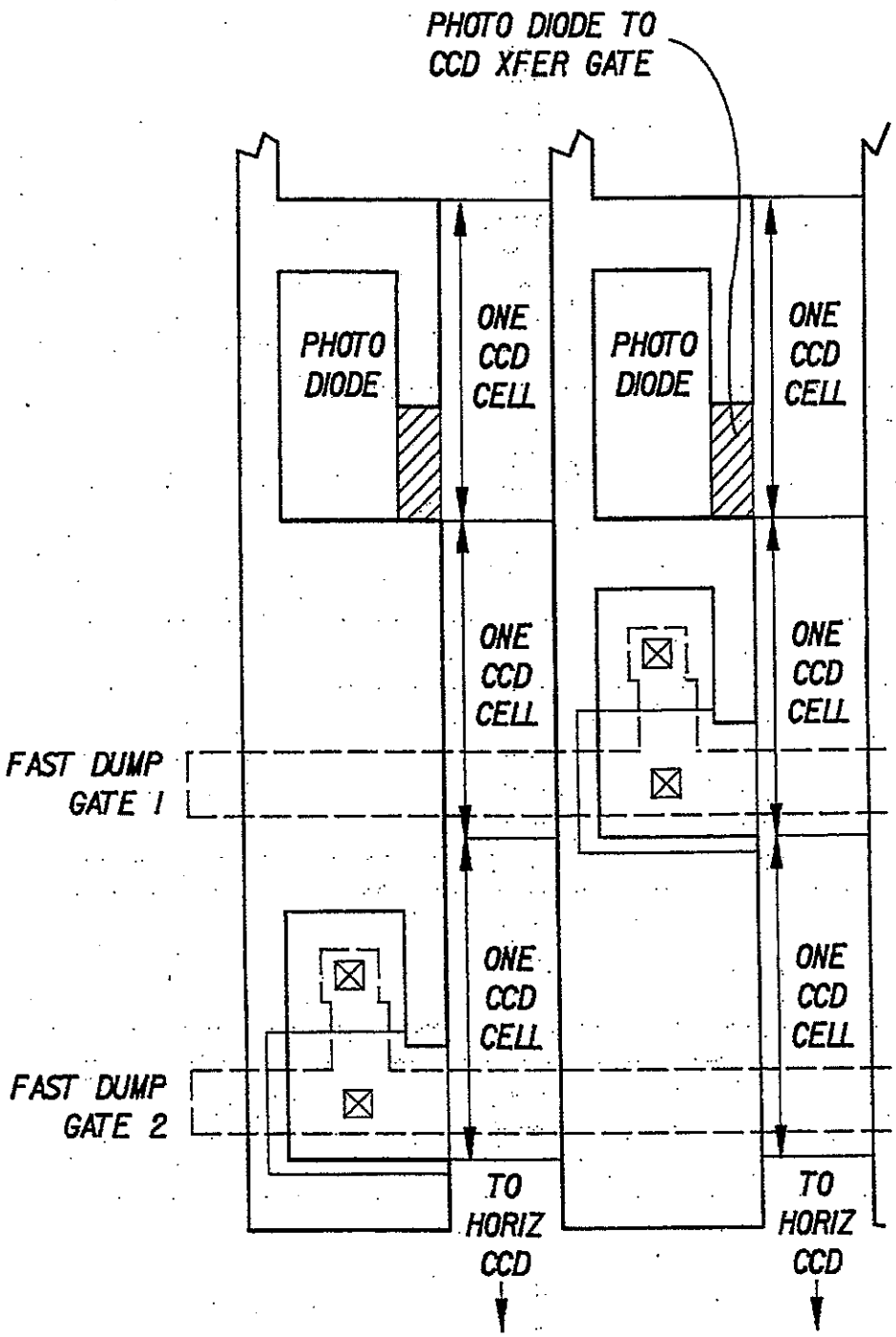



FIG. 10

AXD024524

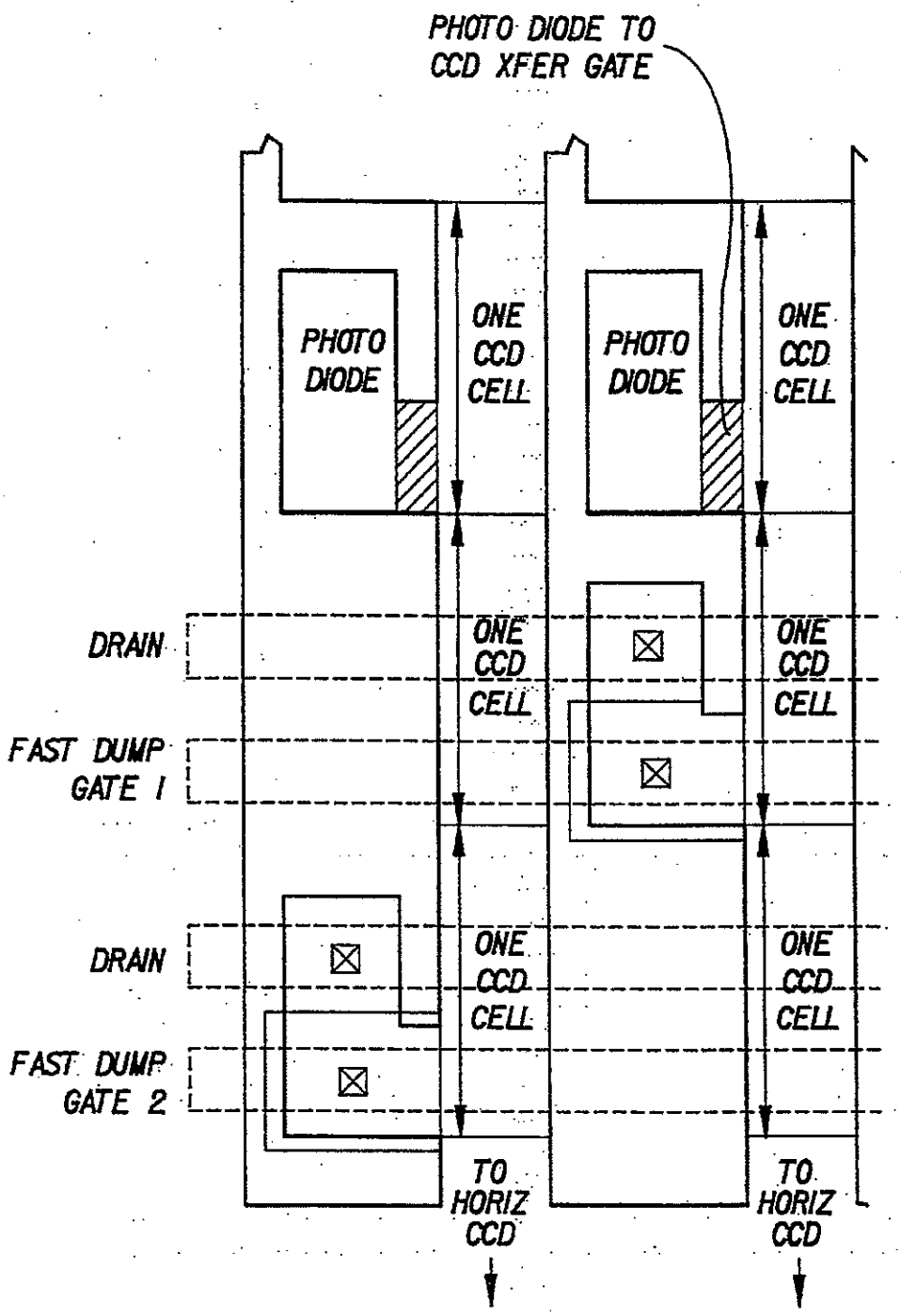



FIG. 11

AXD024525

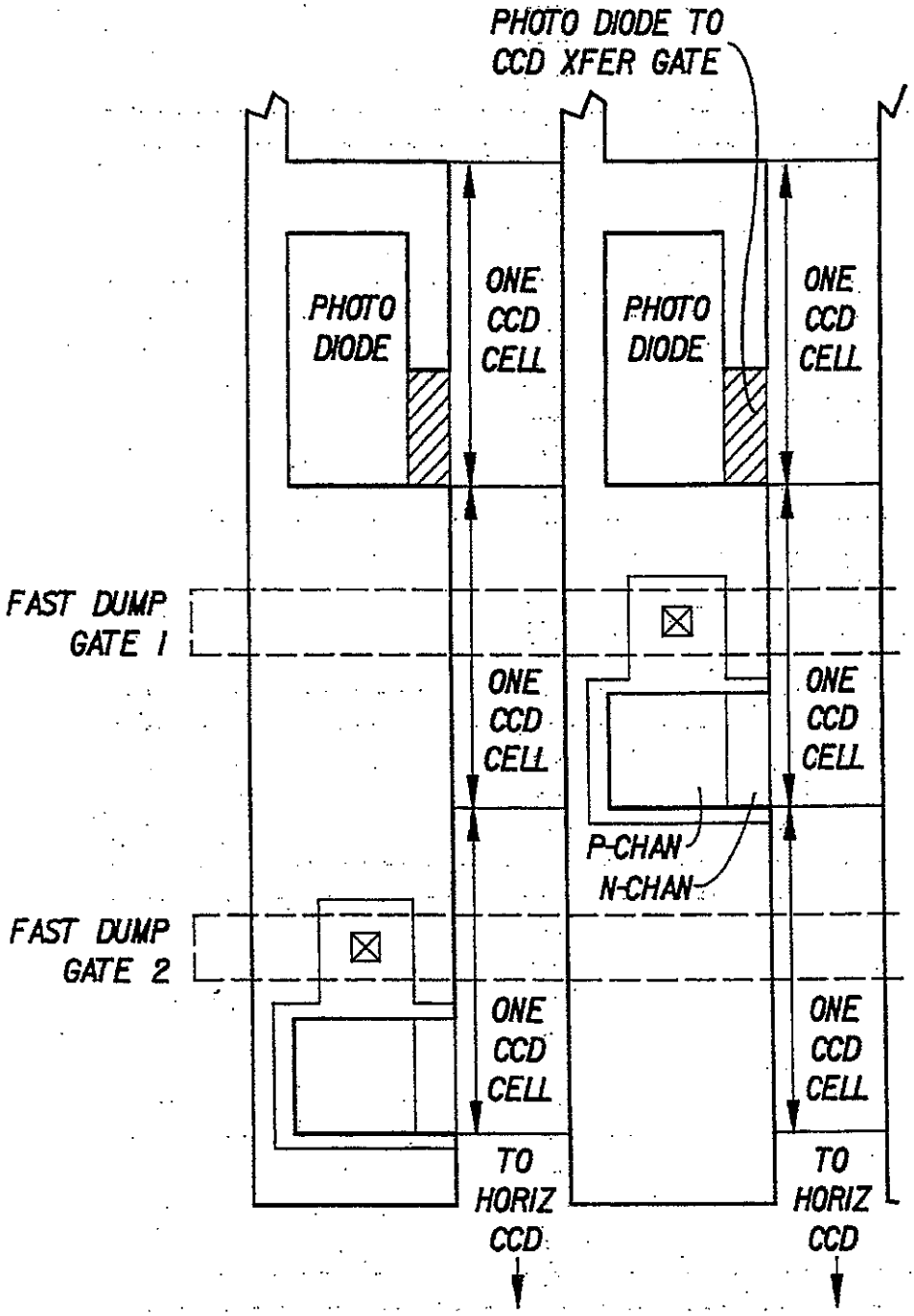



FIG. 12

AXD024526

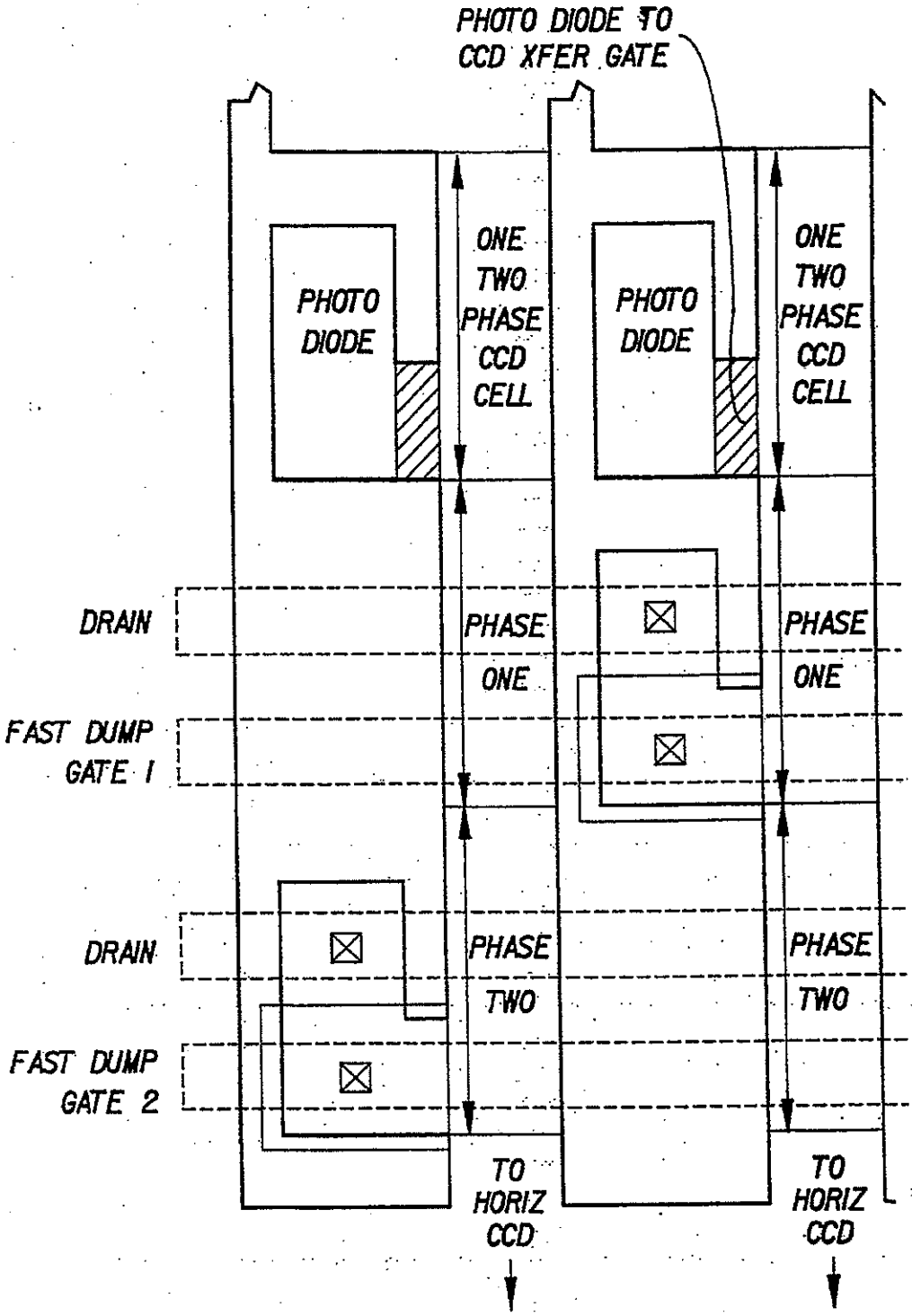



FIG. 13

AXD024527

# MOTION/STILL ELECTRONIC IMAGE SENSING APPARATUS

## FIELD OF THE INVENTION

The invention relates generally to an electronic imaging system. More specifically, the invention relates to an electronic imaging system for capturing images in both a motion mode and a still mode, wherein the electronic imaging system captures medium resolution motion images at a standard frame rate and high resolution still images at a much lower frame rate.

## BACKGROUND OF THE INVENTION

Motion/still electronic imaging systems including the capability of recording analog motion images and digital still images on the same recording medium, for example 8 mm or VHS format magnetic tape, have recently been developed by a number of manufacturers. The motion/still camcorders currently available record motion images in the same manner as conventional motion only video recording cameras. In order to record still images, the user activates an operator control to switch to a "still" mode of operation in which image data generated from the systems electronic image sensor is temporarily stored in a digital memory for subsequent recording onto videotape.

Conventional motion/still camcorders utilize the same type of NTSC resolution interlaced electronic image sensors originally developed for motion only electronic camera systems. Although the conventional image sensors provide sufficient data to produce relatively low resolution analog NTSC signals, the image sensors are not capable of generating still images having the high resolution associated with high quality electronic still imaging systems. Some current electronic still imaging systems, for example, are capable of recording over one thousand lines of image information, while only 480 lines of image information are required for one frame of an NTSC video signal.

Of course, a high definition television (HDTV) electronic image sensor could be used in a motion/still camcorder to directly obtain high resolution still images and HDTV motion images, but downconversion would be required to obtain NTSC motion images. In such a case, the electronic image sensor must be capable of operating at pixel data rates of greater than 50M pixels/second. Electronic image sensors capable of operating at such high pixel data rates, however, are typically very costly to produce and have much higher power consumption rates than conventional NTSC compatible sensors.

In view of the above, it is an object of the invention to provide an electronic imaging system that is capable of producing NTSC motion images and high resolution still images. It is a further object of the invention to provide an electronic image sensor for the electronic imaging system, which can be operated in a low resolution mode to provide NTSC resolution motion scenes at the standard thirty frames/second rate, and operated in a high resolution mode to provide high resolution still images at slower frame rates. It is a still further object of the invention to provide an electronic image sensor, as described above, that is less expensive to produce and has lower power consumption requirements than HDTV electronic image sensors.



## SUMMARY OF THE INVENTION

The invention provides an electronic imaging system that records both motion and still video images. In a motion mode of operation, the electronic imaging system records NTSC resolution images at a standard thirty frame per second rate. In a still mode of operation, the electronic imaging system records megapixel resolution still images at a much lower frame rate.

The electronic imaging system utilizes an electronic image sensor that includes an array of photosensitive picture element sites, or "pixels" which collect photogenerated charge packets. Each charge packet is a pixel image signal. Image signals are generated from all of the pixels in the still mode of operation. In the motion mode of operation, however, the image signals generated from certain selected pixels are discarded or combined with the signals from nearby pixels in order to generate images at thirty frames per second while using a standard video rate output pixel clock (approximately 12 MHz) instead of an HDTV rate pixel clock (>50 MHz). The electronic image sensor incorporates column selective fast dump "charge clearing" structures and column selective "charge parking" structures. The charge clearing structures are used to selectively discard the signal charge from certain color pixels. The charge parking structures are used to sum the charge from non-adjacent vertical pixels. The architecture of the electronic image sensor also allows different image aspect ratios to be provided for the motion and still modes described above.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in greater detail with reference to the accompanying drawings wherein:

FIG. 1 is a block diagram of an electronic imaging system in accordance with the invention;

FIG. 2 illustrates an image pixel site of the type incorporated in the electronic image sensor shown in FIG. 1;

FIG. 3 illustrates a charge clearing structure of the type incorporated in the electronic image sensor shown in FIG. 1;

FIG. 4 illustrates a first embodiment of the electronic image sensor shown in FIG. 1;

FIG. 5 illustrates the use of a different color filter array with the electronic image sensor structure shown in FIG. 4;

FIG. 6 illustrates a charge parking structure utilized in a second embodiment of the invention;

FIG. 7 illustrates an electronic image sensor in accordance with a second embodiment of the invention that utilizes the charge parking structure illustrated in FIG. 6 and the charge clearing structure illustrated in FIG. 3;

FIG. 8 illustrates a third embodiment of the invention that incorporates aspect ratio conversion;

FIG. 9 illustrates a fourth embodiment of the invention that incorporates aspect ratio conversion;

FIGS. 10–12 illustrate three methods of creating column selectable "charge clearing" structures using 2 CCD phases per row; and

FIG. 13 illustrates a "charge clearing structure using 1 CCD phase per row.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A motion/still electronic imaging system according to the invention is illustrated in FIG. 1. The imaging system includes an optical system 10, a motion/still

electronic image sensor **12**, a camera control processor unit **14**, signal processing electronics **15**, a recording unit **16**, and an operator control unit **18**, which includes a mode selection switch **20** and a record or "shutter" control switch **22**. An optional flash unit may also be incorporated in the structure of the imaging system or as an accessory item. The optical system **10** of the illustrated embodiment includes a lens **24**, and an adjustable aperture **26**, which are controlled by the camera control processor unit **14**. It will be understood that the invention is not limited to the use of illustrated optical system **10**, but is also applicable to imaging systems using any type of known optical system, including those using fixed apertures and systems that utilize mechanical shutter devices.

In operation, a user places the mode switch **20** in a "motion" mode position and depresses the record switch **22** to record motion images. The camera control processor unit **14** controls the operation of the electronic image sensor **12**, the signal processing electronics **15**, and the recording unit **16** in order to record the output of the electronic image sensor. The recording unit **16** preferably includes a digital magnetic tape recording unit, so that the processed sensor output signal is recorded on a magnetic tape located in the recording unit **16** as an NTSC resolution video image sequence until the record switch **22** is released. To record a still image, the user places the mode switch **20** into the "still" mode position, so that a high resolution still image is captured and recorded by the recording unit **16** each time the record switch **16** is depressed. The recording unit **16** preferably includes digital memory means for storing the still images (for example Flash EPROM memory cards) in addition to the magnetic tape recording unit, although the still images can also be stored on tape if desired.

The electronic image sensor **12** includes a row and column array of pixels that generate signal in response to the amount of radiation incident thereon and at least one horizontal output register. A conventional color filter array (not shown) is provided so that selected pixel sites generate image signals corresponding to red, green and blue color components. In addition to the photosensitive pixels, the electronic image sensor includes column selective "charge clearing" structures and column selective "charge parking" structures. The charge clearing structures are used to selectively discard the signal charge from certain pixels, while the charge parking structures are used to add the charge from non-adjacent vertical pixels.

FIG. **2** illustrates a top view of one photosensitive pixel of the type included in the array of the electronic image sensor **12**. The pixel is of conventional construction, and is preferably of the type incorporated in the KAI-1001 interline image sensor manufactured by the Eastman Kodak Company of Rochester, N.Y. The design and operation of this image sensor is described in "KAI-1001 series Megapixel Interline CCD Image Sensor Performance Specification," Rev. 1 April 1993, available, from the Microelectronics Technology Division of Eastman Kodak Company, and in "A 1 Megapixel, Progressive-Scan Image Sensor with Anti-blooming Control and Lag-Free Operation" by E. G. Stevens, et al., IEEE Trans. Electron Devices, Vol. 38, May 1991, both of which are incorporated by reference herein. The 9×9 micron pixel site includes a photodiode **30**, a transfer gate **32** and a two-phase CCD register **34**. The operation of the photosite is well known in the art and need not be discussed in great detail.

FIG. **3** illustrates a top view of one of the charge clearing structures incorporated in the electronic image sensor **12**. The charge clearing structures are located in selected columns of at least one row of vertical transfer registers located between the two-dimensional array of photosites and a horizontal output register of the electronic image sensor **12** as will be described in greater detail below. The charge clearing structure includes a fast dump gate **36** and a drain **38** located adjacent to the CCD register **34**. The fast dump gate **36**, when activated, permits charge being transferred in the CCD register **34** to be dumped to the drain **38**. The drain **38** may be a separate electrode, as shown in FIG. **11**, or, as shown in FIG. **10**, it may contact a polysilicon and a metal drain line connected via a bond wire to an external control pin on the sensor package, which is held at an appropriate potential so as to drain the charge from CCD register **34**.

FIGS. **10–12** show different charge clearing structures using one true two-phase CCD cell per row. It is also possible to use charge clearing structures having only one of the two CCD cells per row. This reduces the number of vertical transfer required to transfer the first line of charge from the photosensitive pixel array to the horizontal readout register. FIG. **10** illustrates the use of a surface-channel, fast-dump gate ($V_T>0$) so that the drain may be connected to the gate, thereby saving a pin. FIG. **11** shows a structure providing a separate gate and drain electrode, as would be required for a buried-channel, fast-dump gate ($V_T>0$). FIG. **12** shows a charge-clearing structure of a vertical type wherein the drain **38** lies below the gate (the n-type substrate). FIG. **13** shows a charge-clearing structure similar to that of FIG. **11**, except that the gate **1** row charge clearing structure is adjacent to phase one of a two phase CCD cell, and the gate **2** row charge clearing structure is adjacent to phase two of the same CCD cells whereas in FIG. **11**, each charge clearing structure is adjacent to a two phase CCD cell.

A preferred image sensor architecture incorporating photosensitive pixels of the type illustrated in FIG. **2** and charge clearing structures of the type illustrated in FIG. **3** is shown in FIG. **4**. For purposes of simplification, an array **40** of image pixel sites is shown having just four image lines, although it will be understood that any number of image lines of any desirable length may be employed. The four image lines are separated from a horizontal output register **42** by four rows of vertical transfer registers **44**, wherein each row of vertical transfer registers **44** includes at least one charge clearing structure **46** and a plurality of normal or conventional vertical transfer stages **48**. The charge clearing structures **46** in each row of vertical transfer registers **44** are respectively controlled by "gate 1", "gate 2", "gate 3" and "gate 4" signals supplied by the camera control processor unit **14** illustrated in FIG. **1**. The image pixel sites are arranged in accordance with a Bayer color filter array pattern as described in U.S. Pat. 3,971,065, "Color Imaging Array" by B. E. Bayer, assigned to Eastman Kodak Co. and incorporated herein by reference, with green photosites arranged in a checkerboard pattern and red and blue pixels arranged on alternate lines. The horizontal output register **42** includes a first horizontal transfer register **50** for green image pixel signals and a second horizontal transfer register **52** for red and blue image pixel signals.

In operation, signal charge packets from each of the lines of photoactive pixels are clocked through the four rows of vertical transfer registers **44** including the charge clearing structures **46**. When a given line is clocked from the imaging array into the "gate 1" row of vertical transfer registers **44**, for example, the signal charge from the first and fifth columns of the line is transferred to the drains **38** of the charge clearing structures **46** if the gate **1** signal is activated. In all other columns of the line (for example columns 2, 3, 4, 6, 7) the signal charge is unaffected. If the gate **1** signal is turned off, the charge clearing structures **46** in the gate 1 row of vertical transfer registers **44** are disabled, and the signal charge packets transferred from the array **40** to the gate **1** row are unaffected. By incorporating four "charge clearing" rows having charge clearing structures **46** offset in different columns, it is possible to eliminate all of the signal charge packets from a given image line by turning on the "clear" signals as the line of image pixel signals passes through the gate **1**, gate **2**, gate **3** and gate **4** vertical transfer rows **44**.

In a still mode of operation, all of the charge clearing structures **46** are disabled, thereby allowing all of the signal charge packets to be clocked into the horizontal output register **42**. The green image pixel signals are subsequently clocked out of the first horizontal transfer register **50** and the red and blue image pixel signals are clocked out of the second horizontal transfer register **52**. The color filter array pattern is designed to provide the best image possible in the high resolution still mode of operation.

An NTSC resolution image is obtained in a motion mode of operation by selectively activating the charge clearing structures **46**. As line one of the image passes through the vertical transfer registers **44**, gate **1** is turned off, but gate **2**, gate **3** and gate **4** are turned on. Thus, only the red image pixel signals associated with every other odd column, i.e. columns **1**, **5**, **9**, etc., are transferred to the horizontal output register **42**. The image pixel signals representing the green pixels and the alternate red pixels of line one are drained off by the activated charge clearing structures **46**. In order to read out image line **2**, the gate **4** signal is turned off and the other three signals are turned on, thus passing every other blue image pixel signal to the horizontal output register **42**. Following the transfer of the blue image pixel signals, the second horizontal transfer register is clocked once to put the blue pixels in their proper location. All of the green image pixel signals for the third image line are kept by deactivating all of the charge clearing structures **46** as the third image line is clocked through the rows of vertical transfer registers **44**. The fourth line of image pixel signals can either be eliminated by turning on all four gate signals or can also be passed to the first horizontal transfer register **50** and summed with the green pixels from the other image lines. The next field of the NTSC signal is "staggered" vertically by shifting the sampling by two lines in the vertical direction.

FIG. **5** shows how the same basic image sensor architecture illustrated in FIG. **4** can be used with a different color filter array pattern, for example a "3G" non-interlaced striped CFA, as described in U.S. Pat. No. 4,663,661 "Single Sensor Color Video Camera with blurring filter" by J. S. Weldy and S. H. Kristy, assigned to Eastman Kodak Company and incorporated herein by reference, to generate an NTSC signal. In this example, the red and blue image pixel signals are clocked into the horizontal output register **42** by turning off the gate **1** signal and turning on the gate **2**, gate **3** and gate **4** signals. The second horizontal transfer register **52** is clocked twice before summing. The third and fourth image lines are clocked into and summed in the horizontal output register by turning off the gate **2** and gate **4** signals and turning on the gate **1** and gate **3** signals. The fourth image lines can alternatively be discarded by turning on the gate **2** and gate **4** signals. As in the case illustrated in FIG. **4**, a still mode of operation is obtained by deactivating all of the gate signals.

Referring now to FIG. **6**, a charge "parking" or storage structure **58** is shown including a storage site **54** and a transfer gate or region **56** located adjacent to the CCD register **34**. The charge parking structure **58** is used in conjunction with the charge clearing structure **46** described above in a second embodiment of the invention. In operation, the transfer region **56** of the charge parking structure **58** is activated to transfer a signal charge packet from the CCD register **34** to the storage site **54**. The storage site **54** can be used to sum signals from different non-adjacent rows of the array of pixels.

The charge is stored by setting the channel potential of the storage site **54** to a higher potential than the transfer region **56**, which is likewise at a higher channel potential than the adjacent CCD register **34**. To later sum the stored charge with a non-adjacent row of charge which has been shifted into CCD register **34**, the channel potential of the CCD register **34** must be brought higher than that of the transfer region **56**, which must be higher than that of the storage site **54**. Otherwise, during readout of CCD register **34**, the transfer region **56** is brought to a lower channel potential than in CCD register **34** or the storage site **54** to create a barrier and prevent the transfer of charge between them.

FIG. **7** illustrates an electronic image sensor in accordance with a second embodiment of the invention. The image sensor is shown having four image lines and two rows of vertical transfer registers **60** which include both charge clearing structures **46** and charge parking structures **58**. As in the structure illustrated in FIG. **5**, electronic image sensor also includes a horizontal output register **42** having first and second horizontal transfer registers **50**, **52** as shown in FIGS. **4** and **5**.

In operation, the charge clearing structure **58** location in column four of the gate **2** row, for example, allows the blue pixel values from image line one and image line three to be summed, even though there is a green pixel value between these two blue values. To obtain an NTSC resolution image, image lines **1** and **2** are clocked into the gate **1** and gate **2** rows. In the gate **2** row, the image line **1** blue pixel values from columns **4**, **8**, etc. are parked or stored while the green pixels and the remaining blue pixels are cleared discarded. In the gate **1** row, the green pixels and alternate red pixels are parked while the remaining red pixels are discarded or cleared. Image lines three and four are subsequently clocked into the gate **1** and gate **2** rows. In the gate **2** row, the line **3** blue pixel values from columns **4**, **8** etc. are summed with the line one blue pixel values, while the green pixels and the remaining blue pixels are cleared. In the gate **1** row, the line **4** red pixel values from columns three and seven etc are cleared, while the green pixels and the remaining red pixels are summed with the values in the charge parking registers. Finally, the image pixel signals are transferred into the horizontal output register.

One additional problem with NTSC motion/still systems is that it may be desirable to use different image aspect ratios for the motion and still modes. For example, NTSC uses a 4:3 aspect ratio image, while the requirement for high resolution stills may be a 3:2 aspect ratio as utilized, for example, in the Kodak Photo CD System. The electronic image sensor is therefore required to have a 1024×1536 image array to provide a 3:2 aspect ration, while for the NTSC mode, it might be desirable to use only 960×1280 pixels from the electronic image sensor to provide a 4:3 aspect ratio image.

A method of facilitating the readout of different aspect ratio images is shown in FIG. 8. The structure shown in FIG. 8 utilizes 256 "aspect ratio charge clearing" structures 46' of the type shown in FIG. 3 placed in the end of at least one row of the vertical transfer registers 44, between the image array 40 containing the photosensitive pixels, and the horizontal output register 48. When activated by a signal supplied by the camera control processor unit 14, the aspect ratio charge clearing structures 46' eliminate the signals from the columns at the left side of the image array 40 as the image lines are clocked out. As a result, the horizontal output register 48 does not receive charge from these columns.

It should be noted that there is insufficient time to clock out all of the 256 extra pixels at the end of each NTSC image line, so that charge from these extra pixels would end up at the right hand side of the horizontal readout register 48 without the use of the aspect ratio charge clearing structures 46'. In such a case, this charge would be added to the right side of the next new line of the image causing a serious artifact. The aspect ratio charge clearing structures 46' eliminate the signals from these pixels so that the next image line contains only the proper signal charge, namely, only the 1280 horizontal pixels needed to be clocked out.

A second embodiment that compensates for the differences in aspect ratios is shown in FIG. 9. The second structure utilizes a second auxiliary horizontal output register 49. The second horizontal output register 49 is centered in the middle of the image array 40 and has 256 fewer elements than the normal horizontal output register 48. Aspect ratio charge clearing structures 46' are used to dispose of the charge in the first and last 128 columns of the image array which are not used in the NTSC readout mode.

The invention has been described with reference to certain preferred embodiments thereof. It will be understood, however, that modifications and variations are possible within the scope of the appended claims. For example, the aspect ratio charge clearing structures need not be located within the same row of vertical transfer registers, but can be located in several rows if desired.

## INDUSTRIAL UTILITY

The invention can be utilized in electronic imaging systems to permit high resolution still images to be produced at low frame rates, while also allowing standard NTSC motion image signals to be produced by the same system. The invention is particularly applicable to commercial camcorder devices.

What is claimed is:

1. An electronic image sensor comprising:

a row and column array of photosensitive pixels for generating image pixel signals in response to incident radiation; a horizontal output register; and vertical transfer means for transferring the image pixel signals generated by the photosensitive pixels to the horizontal output register;

wherein the vertical transfer means includes pixel dumping means for selectively preventing the image pixel signals generated in at least one of the columns of each row of the array of photosensitive pixels from being transferred to the horizontal output register;

wherein the vertical transfer means includes a row and column array of vertical transfer registers and the pixel dumping means includes a plurality of charge clearing structures in each row of vertical transfer registers; and

wherein the charge clearing structures of each row of vertical transfer registers are offset in different columns from the charge clearing structures of all other rows of vertical transfer registers.

2. The electronic image sensor of claim 1, wherein the vertical transfer means further comprises charge parking means for temporarily storing signal charge from at least one of the columns of each row of the array of photosensitive pixels, wherein signal charge packets from multiple rows of the array are summed in the charge parking means.

3. The electronic image sensor of claim 1, wherein the horizontal output register includes first and second horizontal transfer registers.

4. The electronic image sensor of claim 1, further comprising an auxiliary horizontal output register, wherein the auxiliary horizontal output register has a shorter line length than the horizontal output register.

5. The electronic image sensor of claim 4, wherein the horizontal output register and the auxiliary horizontal output register each include first and second horizontal transfer registers.

6. The electronic image sensor of claim 1, wherein the row and column array of vertical transfer registers comprises at least four rows.

7. An electronic imaging system comprising:

an electronic imaging sensor; an optical system for imaging scene light onto the electronic imaging sensor; a camera control processor coupled to the electronic imaging sensor; an operator control unit coupled to the camera control processor; and an image data storage unit coupled to the output of the electronic imaging sensor;

wherein the camera control processor controls the electronic imaging sensor to operate in either a still image mode or a motion image mode in response to a mode signal received from the operator control unit;

wherein the electronic imaging sensor comprises a row and column array of photosensitive pixels for generating image pixel signals in response to incident radiation, a horizontal output register, and vertical transfer means for transferring the image pixel signals generated by the photosensitive pixels to the horizontal output register, said vertical transfer means including pixel dumping means for selectively preventing the image pixel signals generated in at least one of the columns of each row of the array of photosensitive pixels from being transferred to the horizontal output register;

wherein the vertical transfer means includes a row and column array of vertical transfer registers and the pixel dumping means includes a plurality of charge clearing structures in each row of vertical transfer registers; and

wherein the charge clearing structures of each row of vertical transfer registers are offset in different columns from the charge clearing structures of all other rows of vertical transfer registers.

8. The electronic imaging system of claim 7, wherein the vertical transfer means further comprises charge parking means for temporarily storing signals from at least one of the columns of each row of the array of pixels, wherein signals from multiple rows of the array are summed in said charge parking means.

9. The electronic imaging system of claim 7, wherein the horizontal output register includes first and second horizontal transfer registers.

10. The electronic imaging system of claim 7, further comprising an auxiliary horizontal output register, wherein the auxiliary horizontal output register has a shorter line length than the horizontal output register.

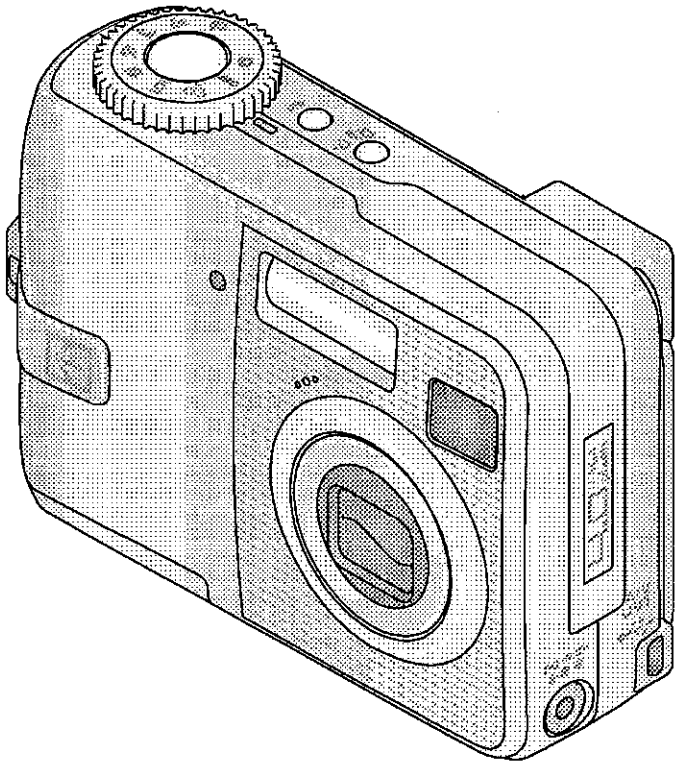
11. The electronic imaging system of claim 10, wherein the horizontal output register and the auxiliary horizontal output register each include first and second horizontal transfer registers.

12. The electronic imaging system of claim 7, wherein the row and column array of vertical transfer registers comprises at least four rows.

* * * * *

# Exhibit 7

# Kodak EasyShare C330 zoom digital camera



# User's guide

www.kodak.com

For interactive tutorials, www.kodak.com/go/howto

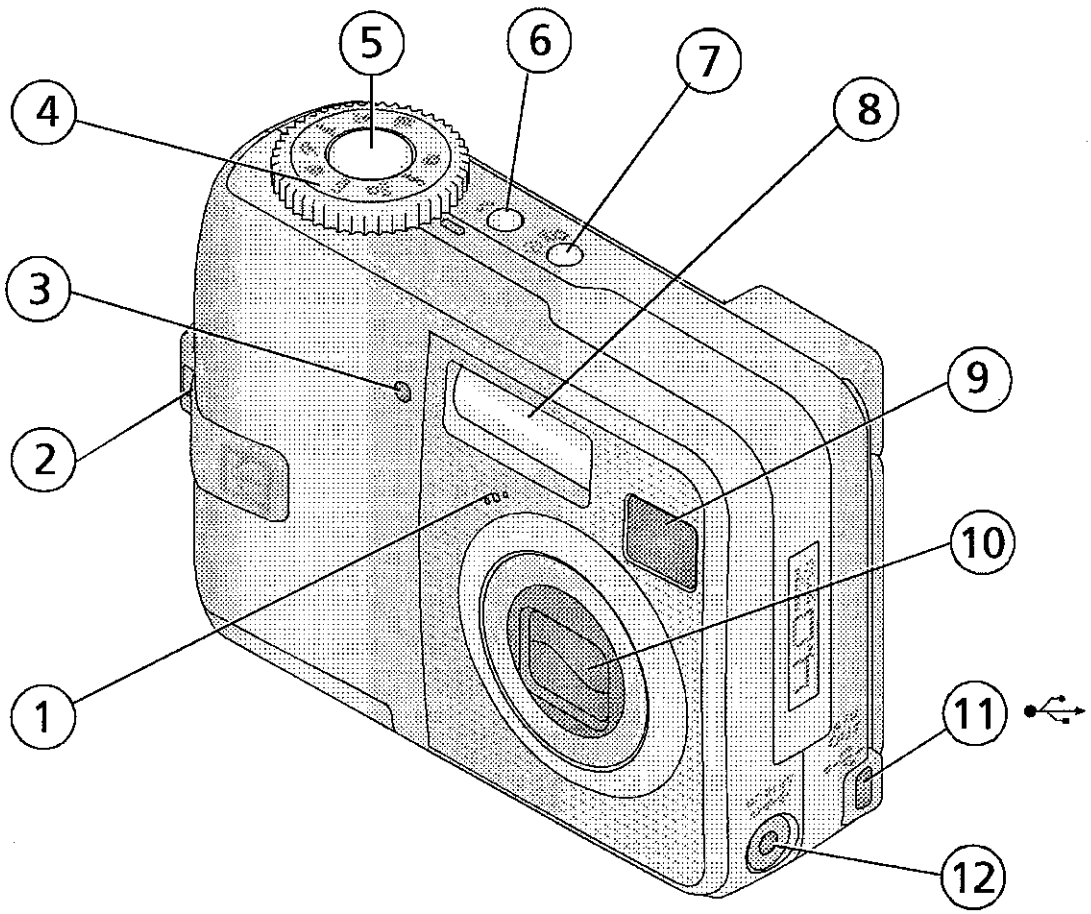
For help with your camera, www.kodak.com/go/c330support

Eastman Kodak Company
Rochester, New York 14650

All screen images are simulated.

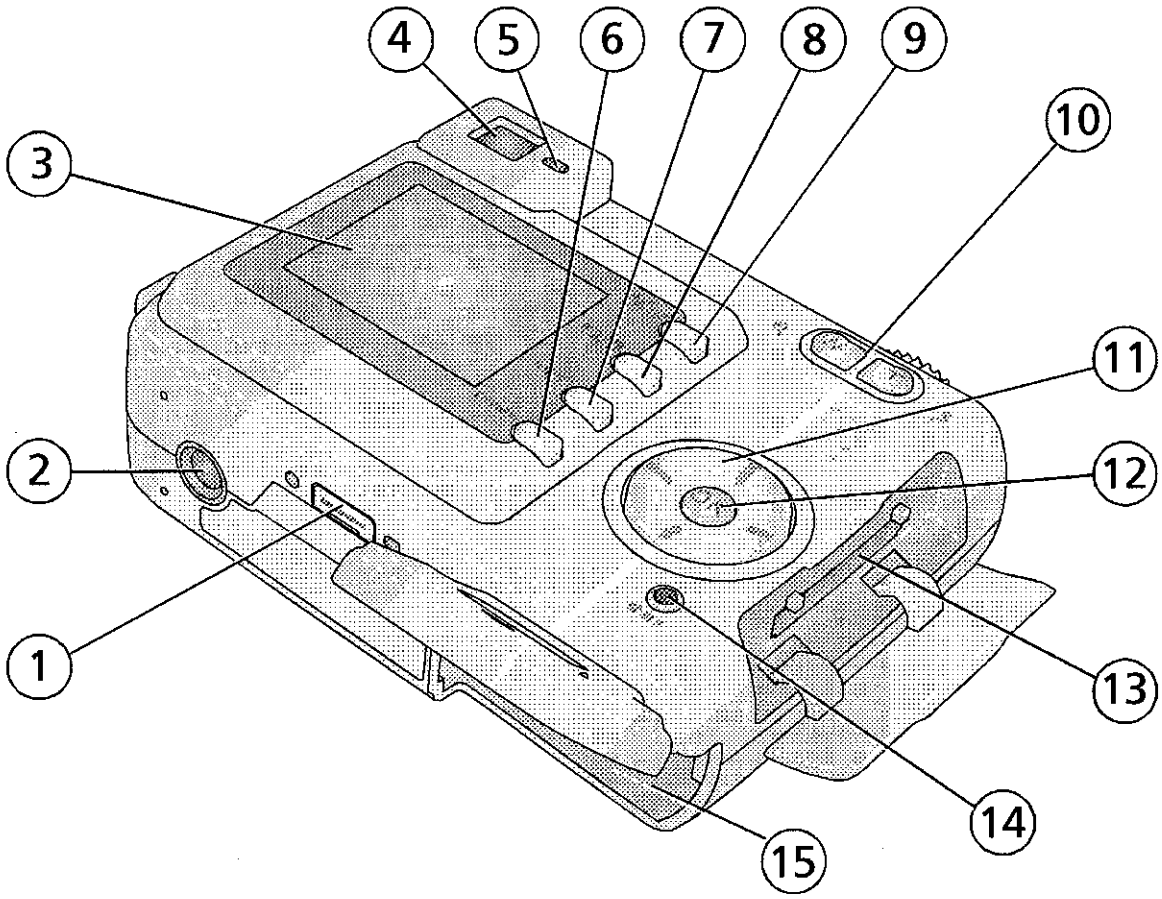
P/N 4J3175

# Front View




| | | | |
|---|---|---|---|
| 1 | Microphone | 7 | Self-timer/Burst button |
| 2 | Wrist strap | 8 | Flash |
| 3 | Self Timer /Video light | 9 | Viewfinder |
| 4 | Mode dial: camera modes/power settings | 10 | Lens |
| 5 | Shutter button | 11 | USB, A/V Out |
| 6 | Flash button | 12 | DC-In (3V) , for **optional** AC adapter |

# Side View




| | | | |
|---|---|---|---|
| 1 | Dock connector | 9 | Delete button |
| 2 | Tripod socket | 10 | Zoom (Wide Angle/Telephoto) |
| 3 | LCD screen | 11 | 4-way controller ◀/▶ ▲/▼ |
| 4 | Viewfinder | 12 | OK button |
| 5 | Ready light | 13 | Slot for optional SD or MMC card |
| 6 | Review button | 14 | Share button |
| 7 | Menu button | 15 | Battery compartment |
| 8 | LCD On/Off/Status ⓘ button | | |

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# Using burst

| Option | Description | Purpose |
|---|---|---|
| **Burst** | Camera takes up to 3 pictures (2 per second) while the Shutter button is pressed.<br>  First 3 pictures are saved. | Capture an expected event.<br><br>**Example:**<br>A person swinging a golf club. |

1 In most Still modes, press the Self Timer/Burst button repeatedly to choose the Burst option.

2 Press the Shutter button **halfway** to set the auto focus and exposure.

3 Press the Shutter button **completely down and hold it** to take the pictures.

*The camera stops taking pictures when you release the Shutter button, when the pictures are taken, or when there is no more storage space.*

NOTE: During Quickview, you can delete all pictures in the burst series. To delete selectively, do so in Review (see page 13).

# Exhibit 8

# United States Patent [19]

**Ryan**

[11] **Patent Number: 4,503,466**

[45] **Date of Patent: Mar. 5, 1985**


[54] **APPARATUS AND METHOD FOR GENERATING OPTIMIZING PICTURES UNDER LOW LIGHT CONDITIONS**


[75] Inventor: **John O. Ryan, Cupertino, Calif.**

[73] Assignee: **Ampex Corporation, Redwood City, Calif.**



[21] Appl. No.: **351,399**

[22] Filed: **Feb. 23, 1982**

[51] Int. Cl.³ ..... **H04N 5/34**

[52] U.S. Cl. ..... **358/211**; 358/219

[58] Field of Search ..... 358/211, 209, 219, 222, 358/243, 310, 312, 313, 332, 345, 346; 315/386



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| 4,340,909 | 7/1982 | Yamada | 358/213 |
| 4,389,610 | 6/1983 | Davidson | 358/211 |



*Primary Examiner*—Tommy P. Chin

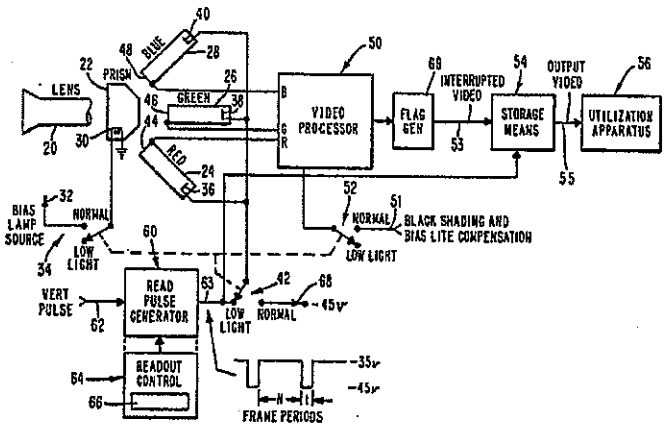
*Attorney, Agent, or Firm*—George B. Almeida; Joel D. Talcott



[57] **ABSTRACT**

The scanning process of a television camera is modified so that scanning is inhibited for N successive scan periods and is enabled during the next scan period, in a repeating cycle of (N+1) periods duration. The signal output generated during the N inhibited scan periods is zero but, during the enabled scan period, is (N+1) times greater than the corresponding signal which would be generated by conventional scanning action.


**8 Claims, 7 Drawing Figures**



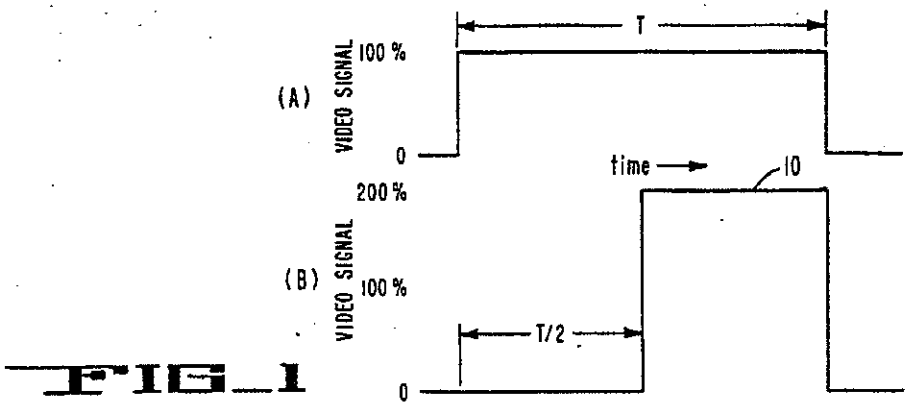



FIG_1

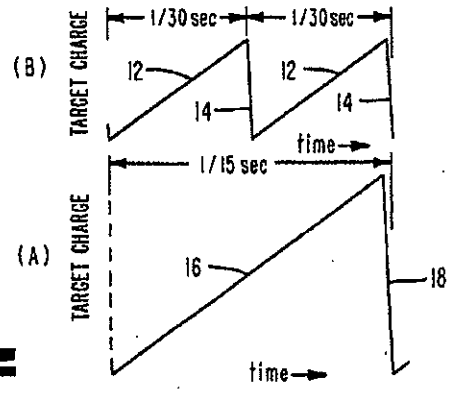



FIG_2

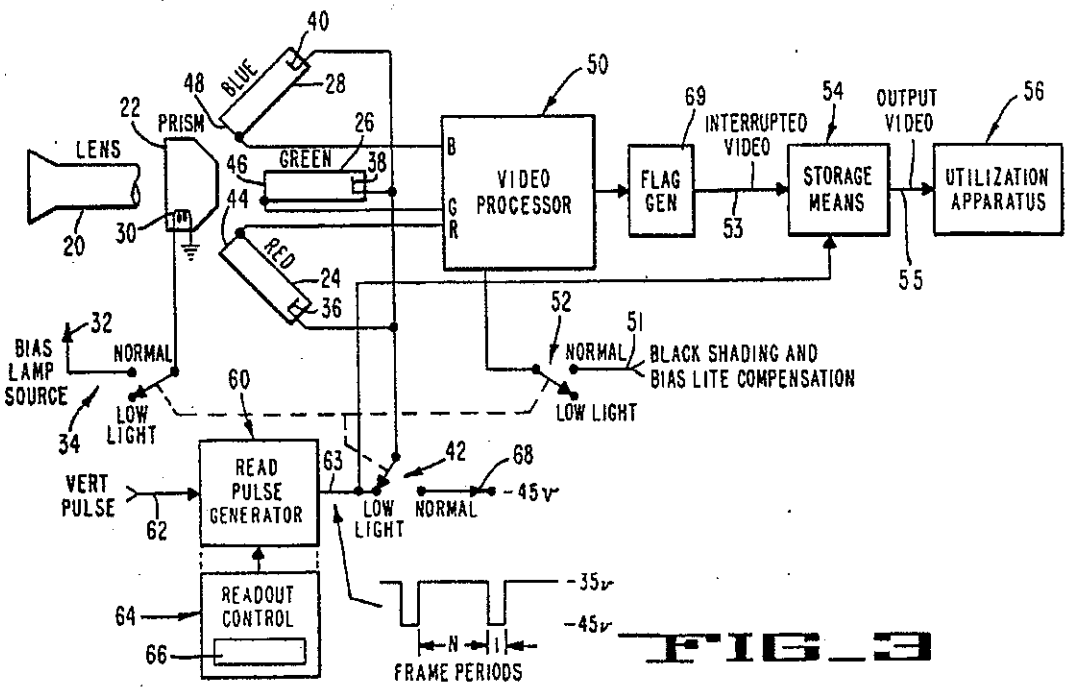



FIG_3

AXD033392

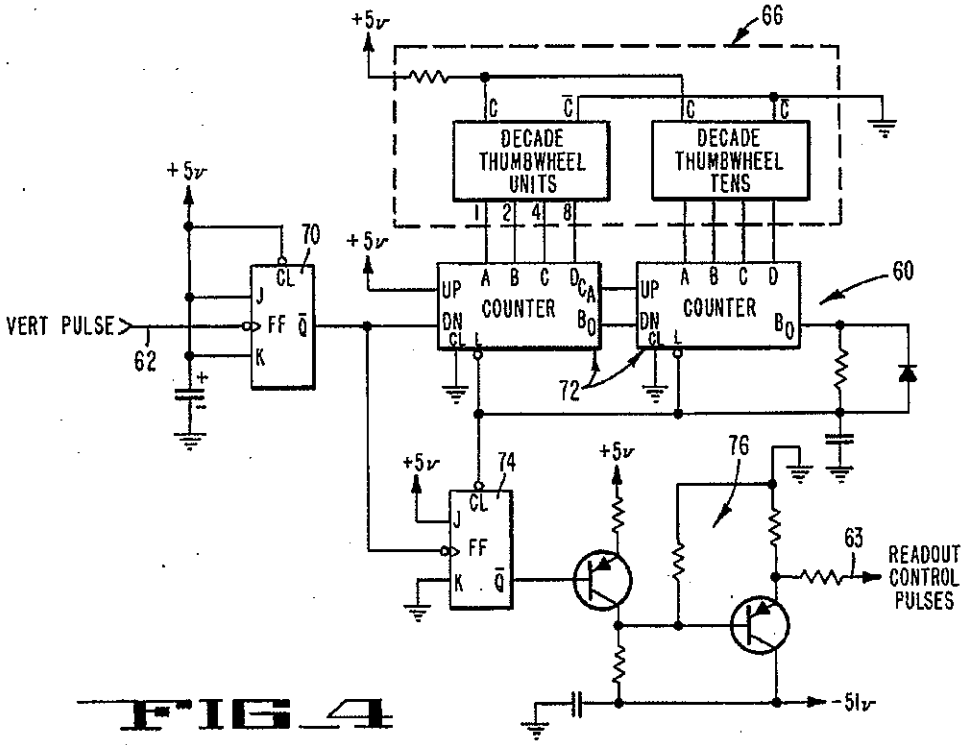

+5v
66
DECADE THUMBWHEEL UNITS
DECADE THUMBWHEEL TENS
1 2 4 8
+5v
70
CL
J
FF Q
K
VERT PULSE
62
UP
DN
A B C D
COUNTER
60
72
+5v
74
+5v
76
63
READOUT CONTROL PULSES
-5lv

FIG_4

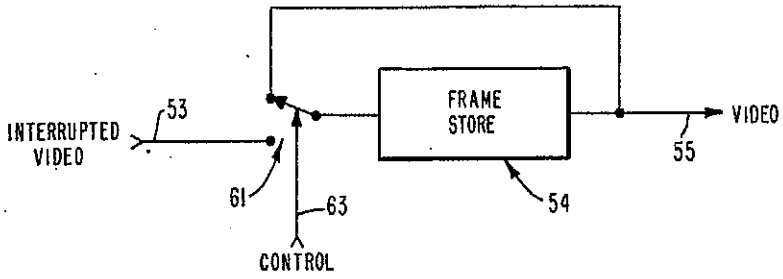

INTERRUPTED VIDEO
53
61
63
CONTROL
FRAME STORE
54
VIDEO
55

FIG_5

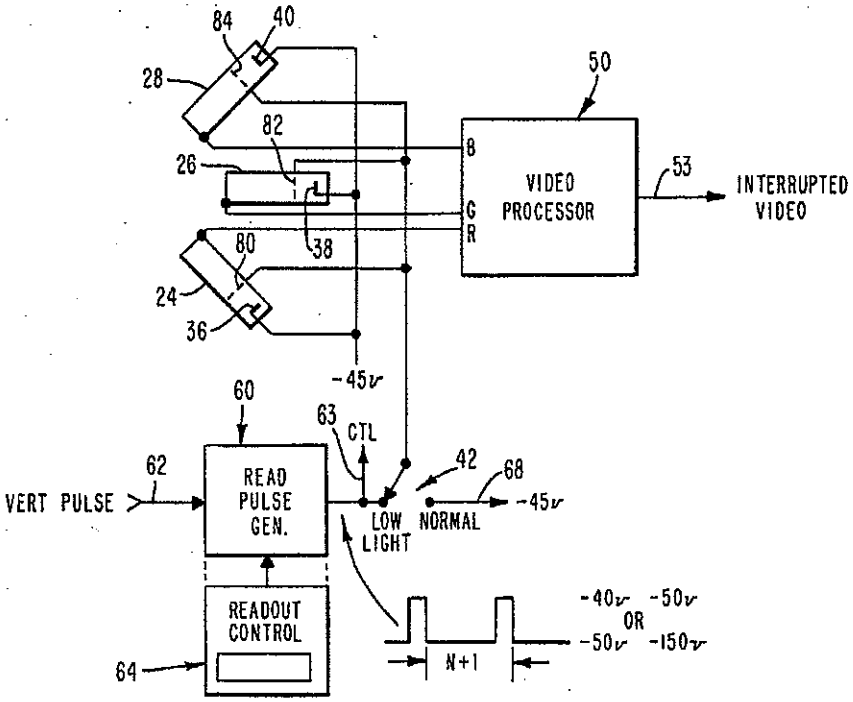



FIG_6

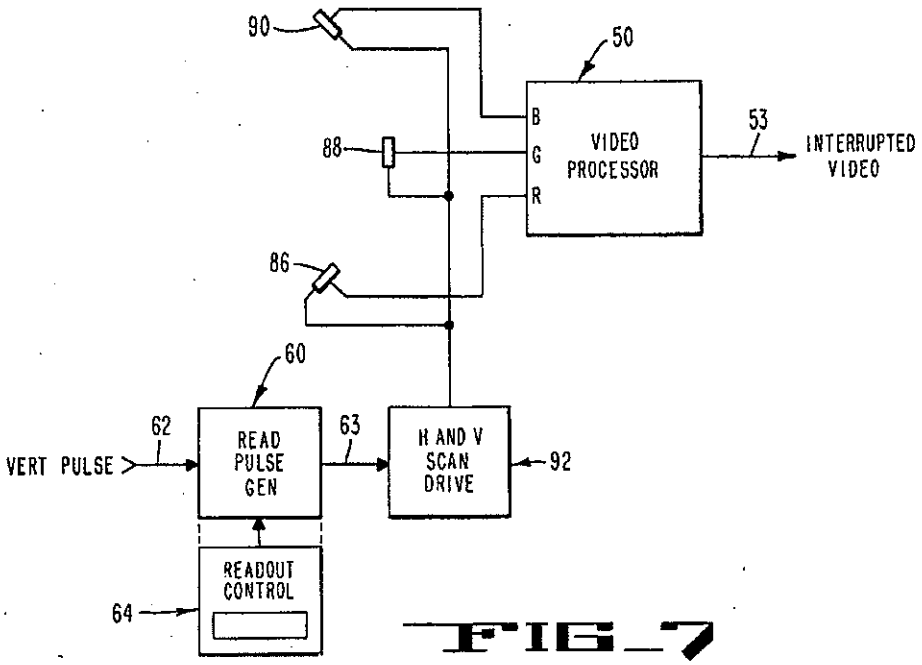



FIG_7

AXD033394

# APPARATUS AND METHOD FOR GENERATING OPTIMIZING PICTURES UNDER LOW LIGHT CONDITIONS

## BACKGROUND AND SUMMARY OF THE INVENTION

The invention relates to means for generating a high quality picture under very low ambient light conditions, and particularly to apparatus and method for producing high quality monochrome or color television pictures under conditions of very low ambient illumination.

In the field of television, and particularly in the fields of electronic news gathering (ENG), electronic field production (EFP), surveillance, etc., there are many instances such as, for example, under twilight or heavy overcast conditions, wherein television cameras cannot be utilized successfully due to the lack of sufficient ambient light to allow recording a scene. Under such low light level conditions, news gathering or other activities using television cameras are precluded, thereby limiting outdoor use of television cameras to daylight hours, or at best, early evening situations. Likewise, closed circuit surveillance systems are limited generally to indoor or outdoor applications where there is sufficient artificial lighting to allow the use of conventional industrial television cameras.

The only known low light level cameras are various types of highly specialized surveillance devices as those used, for example, by the military. Such devices are generally monochrome systems using special image intensifier tubes, are very expensive, and under normal illumination conditions are generally incapable of making color television pictures of a quality suitable for broadcast purposes. Thus such specialized devices can be used only for their intended purposes.

The invention overcomes the shortcomings of the above mentioned devices, by providing a relatively simple system for producing high quality moving or still color television pictures, under conditions of very low ambient illumination. Further, the system is applicable to present high quality cameras utilizing conventional image pickup tubes, which cameras inherently are capable of, and intended for, generating broadcast quality pictures under normal light level conditions. Thus a particularly valuable and heretofore unavailable application of the invention combination is in the field of electronic news gathering. An ENG camera with the capability of readily being switched to a low light level mode of operation permits the capture of newsworthy events which occur outdoors in deep twilight. At present, this has been well outside the capability of all existing ENG, or of all EFP cameras. As further described below, the primary drawback of the system is that the video signal is "interrupted"; i.e., the resulting pictures which are generated do not occur at the usual frame rate, and thus are discernable by a viewer as successive pictures of the scene. However, in accordance with the invention combination, various schemes are contemplated for generating continuous video pictures from the interrupted signal. In any event, when newsworthy events occur, successive periodic pictures of the scenes are far preferable to not being able to obtain any pictures at all.

Accordingly, the invention combination utilizes the principle that the signal current generated by a television image tube, or other similar sensor, throughout a specific time interval corresponding to a specific area of the imaged scene, is directly proportional to the corresponding illumination level on the sensor and to the integration time, i.e., to the period between successive scans of the specific area. In conventional television cameras, the integration time is fixed and is equal to the reciprocal of the picture repetition frequency, i.e., to the frame frequency (1/30 of a second in the NTSC color television standard, and 1/25th of a second in the PAL standard). In the invention combination, the scanning process used in a television camera is modified to inhibit scanning for N successive frames and to enable scanning during the next frame period, in a repeating cycle of (N+1) frames duration. It follows that the signal output from the sensor during the enabled, or "on", frame will be (N+1) times larger than the corresponding signal generated by conventional scanning action. However, the signal output is zero for the N inhibited, or "off", frames, thereby providing the interrupted video signal.

The interrupted video signal may be selectively manipulated to optimumize the final output video signal, depending upon the medium in which the video is to be used, the type or content of the video signal desired, etc. By way of example, the video signal from the camera may be recorded on a suitable video recorder and subsequently replayed in the "still frame" mode. Alternately, the video signal may be fed to a frame store, wherein the gaps in the interrupted video signal corresponding to the inhibited frames can be filled in with video generated during an adjacent enabled frame.

Accordingly, it is an object of the present invention to provide a system and method for producing high quality monochrome or color pictures under very low ambient light conditions.

It is another object to provide quality television signals under low ambient light conditions utilizing generally conventional cameras with conventional image pickup tubes.

It is still another object to provide quality television pictures in a television camera by selectively inhibiting and enabling the readout of given frames of information in a repeating cycle of frames generated by the camera.

Another object is to inhibit the readout of given frames in a repeating cycle of frames by selected manipulation of given elements of the scanning devices.

A further object is to provide optimum still or moving television pictures in low light conditions while still providing broadcast quality television signals during normal light level conditions.

A still further object is to optimize the effective sensitivity of an optical-to-electrical transducer under low ambient light level conditions.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A–1B is a graph illustrating video output signals for a camera without and with the invention system. FIGS. 2A–2B is a graph illustrating the charges on a given small portion of a target without and with the invention system.

FIG. 3 is a block diagram depicting one implementation of the invention combination.

FIG. 4 is a schematic diagram illustrating in further detail the block diagram of FIG. 3.

FIG. 5 is a block diagram exemplifying frame store apparatus for use in the system of FIG. 3.

FIGS. 6 and 7 are block diagrams of alternative embodiments of the invention combination.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

For simplicity of description, it is assumed that a television camera is directed at a perfectly white chart, and thereby produces a constant white level video output signal, such as depicted in FIG. 1A. Given a signal of an undefined period of time T, if the area under the curve is effectively measured, it defines the total light that impinges the camera lens and the target of the tube thereof for that period of time T. Thus the signal may vary from zero at the base line, to 100% at its white level for the time period T.

If the scanning action is altered such that there is no readout during the first half of the time period T (FIG. 1B), and then there is readout during the second half of the period T, the resulting video signal 10 is zero for the first half and is twice the value of the 100% video signal for the second half of the period T. However, the area under the curve of the FIG. 1B is identical to that under the curve of FIG. 1A. Thus it may be seen that the signal generated on the target of the tube is dependent upon the intensity of the light and also upon the amount of time the light fell on the target.

In conventional television camera operation, the incoming light falls on the target for one frame (i.e., 1/30 second in the NTSC color television standard), whereupon the electron beam reads out (i.e., scans) the signal charge on the target for each frame to provide the corresponding television signal at 30 frames/second. In this case, the light has 1/30 of a second to build up an image on any given portion of the target.

Referring to FIG. 2A, it follows that for a constant amount of incoming light the charge at the given portion of the target builds up linearly as a function of time as depicted at numeral 12, since the light is falling constantly with time. After 1/30 of a second, the charge is read out and the video signal drops to zero value, as depicted at numeral 14. Thereafter the charge builds up again during the next 1/30 of a second, is read out again, etc., throughout a conventional scan process.

Referring to FIG. 2B, if the integration period is altered as discussed in FIG. 1B, to enable readout for only one frame out of two, the charge at the given portion of the target builds up to twice the value, as depicted at numeral 16, since the light is falling on the target for twice the amount of time. The target then is read out by the scanning beam after, for example, 1/15 of a second, as depicted at numeral 18.

In the situation of FIG. 2B, the resulting signal generated by the cameras is an interrupted video signal, viz, the camera output is a single flash of 1/30 second corresponding to a frame of information, i.e., a color television picture, followed by 1/30 second of darkness, followed by another 1/30 second flash of a single frame, followed by 1/30 second of darkness, etc. Therefore, the increase in effective sensitivity, viz, the doubling of the light level of the generated pictures, is accomplished at the expense of being able to obtain only one image in 1/15 second, instead of two images as would be generated in the conventional scan method of FIG. 2A.

Referring to FIG. 3, a simplified television camera system is depicted to illustrate the invention combination, and includes conventional lens apparatus 20, prism apparatus 22 for splitting the light supplied by the lens 20, and red, green and blue camera pickup tubes 24, 26, and 28 for receiving the separated light. Prism 22 is depicted herein as including a conventional bias light arrangement 30, which is coupled to a bias lamp source 32 via a switch 34, and operates in conventional fashion to flood the faceplate of the tubes to correct for lag effects. The cathodes 36, 38, 40 of the tubes 24, 26, 28 respectively, are coupled to the common side of a switch 42. The targets 44, 46, 48 of the tubes supply the red, green and blue color television signals, and are coupled to conventional video processor circuitry 50. Conventional black shading, bias light, etc., compensation circuitry, indicated by numeral 51, is coupled to the video process circuitry 50 via a switch 52. The compensation circuitry conventionally cancels out various detrimental effects on the video signals due to the bias light, black shading, etc.

The interrupted video signal supplied by the processor circuitry 50 herein is shown coupled via a line 53 to video storage means 54 such as, for example, a frame store, etc. The final output video signal is subsequently selectively supplied via a line 55 to a suitable utilization apparatus 56 such as, for example, a monitor, print-out apparatus, photographic camera, etc. The apparatus of storage means 54 and/or the utilization apparatus 56 is determined by the particular use to which the camera system is put.

A read pulse generator 60 receives a vertical sync pulse from the camera system sync generator (not shown) via an input 62 and generates therefrom read control pulses of selectable frequency on a read control line 63. The frequency of the control pulses is determined herein, by way of example only, by the setting on a read frequency control means 64, typically a pair of decade thumbwheels 66 (FIG. 4). Thus the read pulse generator 60 and read frequency control means 64 define a readout control means which inhibits or enables the scanning beam to readout the target, in response to the thumbwheel settings. A number corresponding to the desired readout frequency is dialed on the thumbwheels 66, as further described in FIG. 4. The generator 60 provides the read control pulses via line 63 to one side of the switch 42, and to a control input to the storage means 54 to control input to the storage means 54 to control the cycling of the pictures fed to the storage means. A second side of switch 42 is coupled to a −45 volt source 68 conventionally supplied to the cathodes of the tubes when the camera system is in normal operation. The switches 34, 42, 52 are mechanically connected to switch together.

In operation, when low light level camera operation is desired, switches 34, 42, 52 are switched to the low light level positions shown in FIG. 3. The bias light 30 is turned off since the light generated thereby generally would overpower the low light level from the scene. The compensation circuitry thus is no longer required, and also is disconnected. The cathodes 36, 38, 40 normally coupled to the −45 volt sorce, are coupled instead to the read pulse generator 60, which supplies pulses which vary in amplitude between −35 and −45 volts, at a frequency determined by the setting dialed on the thumbwheels 66. When the cathodes are at −35 volts the readout process is inhibited and the tubes integrate the incoming light. When the cathodes are at −45 volts the readout process is enabled and the target charges are read out to provide the red, green and blue color signals.

More particularly, when the read control signal is at −45 volts, the electron beams of the tubes are allowed to read out the respective targets. When the cathodes are pulled up to −35 volts, no further electrons will

land on the target, readout is inhibited, and the target is allowed to build up charges corresponding to the time duration and the incoming light levels of the scene.

Thus, when the scanning process in a television camera is modified, for example, via the circuit of FIGS. 3, 4, scanning readout is inhibited for N successive frames and is enabled during the next frame, in a repeating cycle of (N+1) frames duration. The signal output from the tube or sensor is zero for the N inhibited frames, and during the enabled frame is (N+1) times larger than the corresponding signal which would be generated by a conventional scanning process. The interrupted video signal is then utilized via the storage means 54 and utilization apparatus 56 of FIG. 3.

More particualrly, the storage means 54 may be a videotape recorder in which the signal is recorded. In subsequent replay, the recorder is operated in the still frame mode whereby the interrupted signals generated by the camera system during the corresponding enabled frames are reproduced indefinitely as successive still pictures, can be fed to a print-out apparatus 56 and printed in the form of hard copies, photographed via a film camera, etc.

In an alternate system, the interrupted signals from the camera system are fed to a frame store, as depicted further in FIG. 5, whereby the inhibited frame time gaps are filled in with the video generated during the previous enabled frame. Thus, the frame store defining the storage means 54 is essentially any device which provides a one-frame delay of digital memory elements. A frame store switch 61 is inserted at the input to the frame store, whereby the output may be fed back to the input thereof. When the frame store is filled with one picture via line 53, the switch 61 coupled the output to the input of the frame store, whereupon the output video is a continuous succession of the stored picture at the normal frame rate. The switch 61 may be controlled, for example, via the leading edges of the read control pulses on line 63. Operation of the frame store 54 may be performed automatically by inserting a suitably timed flag pulse of, for example, a few microseconds length, in the vertical interval just preceding an enabled frame, thus instructing the frame store to enter the "write" mode. In FIG. 3, the flag pulse is inserted in the video signal via a flag pulse generator 69, shown herein as inserted in the output of the video processor circuitry 50. Since the insertion and detection of the flag pulse is conventional, no further description is provided.

The use of a frame store effectively captures the scene as a series of still pictures which occur every (N+1) frames. For small values of N, the effects of motion are reasonable well captured, and of course the effective increase in camera sensitivity is correspondingly small. Larger values of N provide correspondingly larger increases in camera effective sensitivity, however any motion in the viewed image which occurs during the (N+1) frames causes blurring in the resulting pictures fed to the storage means 54.

FIG. 4 exemplifies an implementation of the read pulse generator 60 and the read frequency control means 64 of FIG. 3. The circuit is essentially a counter with a controllable output pulse frequency determined by the settings dialed on the decode thumbwheels 66. That is, the pulse generator 60 supplies an output pulse which is low, i.e., −45 volts, for one frame out of (N+1) frames, wherein the thumbwheels are set at (N+1). To this end, the vertical sync pulse on input 62 is divided by two in a JK flip-flop 70 to provide one pulse per frame. The output is fed to a counter 72, which counts the incoming pulses and generates via a JK flip-flop 74 a single read control pulse output every (N+1) frames. Transistors 76 provide means for transforming the logic level signals of, e.g., 5 volts of the counter to the levels required for driving the tube elements.

Thus if the number 10 is dialed on the thumbwheels, the counter 72 generates one read control pulse of −45 volts for every 10 incoming pulses; a 10-to-1 integration sequence, which provides pictures with 10 times the light of a conventional scan process. If the number 30 is dialed on the thumbwheels 66, one read control pulse is generated for every 30 incoming pulses, with a 30-to-1 integration sequence.

The thumbwheels 66 can be set at numbers ranging, for example, from 2, 3, 4, 5, . . . 15, 20, 30 (corresponding to one picture every second) 60, and even up to 90 (corresponding to one picture every three seconds). To date, useful pictures have been obtained with integration times of from 1/15 to one second, where one second times correspond to five F-stops of extra sensitivity.

Referring now to FIG. 6, an alternate method and circuit for modifying the camera readout process in accordance with the invention, is illustrated. Instead of controlling the cathodes, in the circuit the scanning beam is turned off by driving the grids 80, 82, 84 of the tubes with a suitable pulse. Thus, for example, in a diode-gun type of pickup tube, the read pulse generator 60 supplies read control pulses which vary from −50 volts to inhibit readout, to −40 volts to enable readout. In a conventional pickup tube, the read control pulses vary from −150 volts to inhibit readout, to −50 volts to enable readout. As shown, the cathodes 36, 38, 40 are coupled to −45 volts.

FIG. 7 depicts another method and circuit for modifying the scanning process in accordance with the invention, wherein the image tubes of the prior circuits are replaced with solid state sensors 86, 88 and 90. In this system, the prior switch 42 comprises generally conventional horizontal and vertical scan drive circuit 92. Readout is controlled by interrupting the horizontal or vertical, or both horizontal and vertical, scan drive signals to inhibit readout during the N frames, and enable readout during the (N+1) frame. The H and V scan drive 92 is coupled to the read pulse generator 60, and is controlled by the read control pulses on line 63.

Although there are various schemes for controlling the readout process as described herein, control of the cathode potential as in FIG. 3 is advantageous since such scheme allows the tube or sensor to read out, and thus suppress, highlights in the scene. That is, if a highlight has a sufficiently high light level to develop greater than 10 volts of charge on the target, it will be read out continually during the scanning process. This prevents excessive light from a street lamp, flashlight, etc., from spoiling pictures which otherwise would be obtainable using the low light level techniques described herein.

Several limiting factors exist in the present system. For example, dark currents are generated in the photosensitive layer of the target. Also stray light from the tube's heater filament may impinge the rear of the target. Further, integration of light over too long a time period may cause excessive blur in the pictures if there is any movement in the scene being viewed. The first two effects may be offset by cancellation techniques

generally known in the art. Further, the dark current may be reduced by using a lower target voltage, and filament light leakage may be eliminated by employing relatively simple optical techniques to block the light. Excessive blurring is minimized by using values of N which are as small as possible, consistent with amount of reduced light available at the scene.

Although the invention combination has been described herein with respect to color television cameras, associated video storage apparatus and the field of color video in general, it is to be understood that the techniques and circuits are useful in any application or field wherein objects, images, etc., are viewed, scanned, etc., by means of, for example, optoelectrical transducers or sensors, whether tube or solid state, which are capable of being activated and inactivated, or otherwise controlled to allow selection of the amount of light which is collected prior to readout of a representative signal. Likewise, the storage means 54 may be any device capable of storing the information corresponding to the generated signal, and of selectively retrieving the information as desired; e.g., a tape or disk recorder/reproducer, a monolithic memory, i.e., frame or picture store or delay device, etc. Further, the invention may be used in cameras with any number of tubes, or which employ solid state image sensors rather than tubes.

What is claimed is:

1. System for increasing the effective sensitivity of an image tube during its readout scanning process, including means for inhibiting the image tube's readout scanning process for a selected plurality of inhibited scan periods of a given repeating cycle of scan periods, and for enabling the image tube's readout scanning process for a selected enabled scan period to generate a corresponding image tube output signal, comprising:

recorder means including a videotape recorder for storing the output signal as successive pictures during the enabled scan period; and

means integral with the videotape recorder for reproducing each successive picture in a still frame mode of operation during respective inhibited scan periods following each enabled scan period.

2. System for generating an optimized picture under very low ambient light conditions, the system including means for the readout scanning of a photosensitive surface, and means for enabling the means for the readout scanning of the photosensitive surface for an enabled scan period out of a selected cycle of scan periods, comprising:

read pulse generator means for generating readout control pulses to initiate the enabled scan period, wherein the absence of readout control pulses from the read pulse generator means inhibits the means for the readout scanning of the photosensitive surface;

solid state image sensor means defining said photosensitive surface;

scan means integral with the means for the readout scanning, for generating a horizontal and vertical scan raster on the solid state image sensor means photosensitive surface; and

wherein readout scanning of the photosensitive surface occurs during the enabled scan period.

3. A circuit for optimizing the effective sensitivity of an image tube having a repeating cycle of scan periods, comprising:

a cathode element;

source means for providing reference sync pulses at a rate corresponding to a television frame rate;

read pulse generator means coupled to the source means for selectively supplying to the cathode element readout control pulses having a potential sufficient to enable readout only for a selected scan period of the repeating cycle of scan periods;

processor means coupled to the tube for receiving a signal therefrom in response to the readout control pulses having said sufficient potential and for providing a corresponding interrupted output signal; and

recorder/reproducer means coupled to the processor means for selectively storing the interrupted output signal and for selectively reproducing the previously stored interrupted output signal to define a corresponding succession of still pictures.

4. The system of claim 3 wherein the recorder/reproducer means include frame store means for storing the interrupted output signal as one frame of information, and for selective reproduction of the one frame during the repeating cycle of scan periods wherein the readout control pulses do not have a potential sufficient to enable readout.

5. The system of claim 3 further including:

means coupled to said processor means for generating a flag timing pulse indicative of the occurrence of the readout control pulses; and

wherein said recorder/reproducer automatically is responsive to the flag timing pulse to selectively store the interrupted output signal.

6. The circuit of claim 3 wherein the read pulse generator means supplies the readout control pulses as a cathode potential of the order of −35 to −45 volts during the selected scan period of the repeating cycle of scan periods.

7. The circuit of claim 3 wherein the read pulse generator means includes;

frequency control means for determining the frequency of the readout control pulses commensurate with a selected range of numbers of the order of from 2 through 90 representative of the repeating cycle of scan periods; and

counter means coupled to the source means and responsive to the frequency control means to generate the readout control pulses.

8. A method for increasing the effective sensitivity of an image tube during a readout scanning process, comprising;

inhibiting the readout scanning process of the tube for a selected plurality of inhibited scan periods;

allowing the integration within the tube of incoming light during the plurality of inhibited scan periods;

enabling the readout scanning process for an enabled scan period following the inhibited scan periods;

the step of enabling further comprising controlling the tube's cathode potential to allow readout thereof as an enabled signal only during the enabled scan period;

storing the enabled signal during the enabled scan period; and

reproducing the enabled signal during the inhibited scan periods to define a succession of still pictures.

* * * * *